

# 功率MOSFET: 从原理、特性到应用分析

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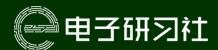
# 主要内容

• 功率MOSFET的原理

• 功率MOSFET的参数和特性

• 功率MOSFET的开关过程分析

• 功率MOSFET的典型应用分析



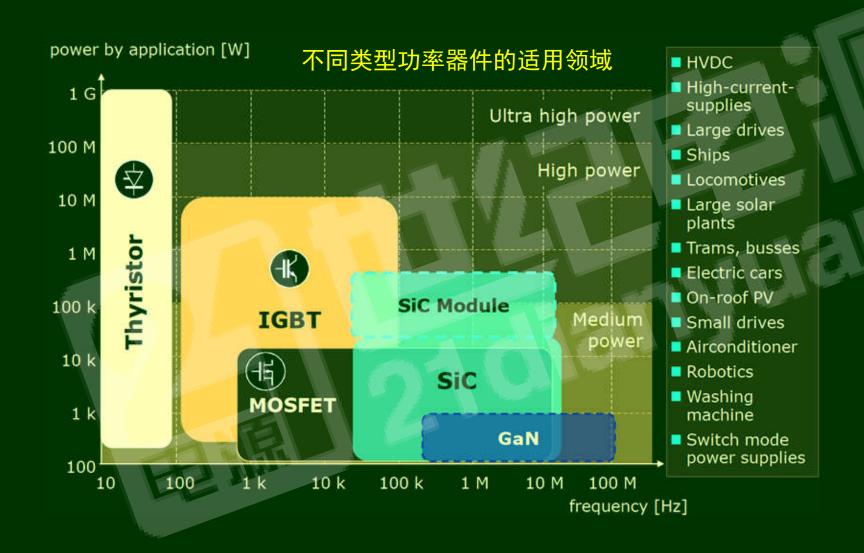
### 功率半导体器件分类

▶电力电子器件(power electronic device)——在电路中,实现 电能的变换或控制的电子器件。





#### 市场需求



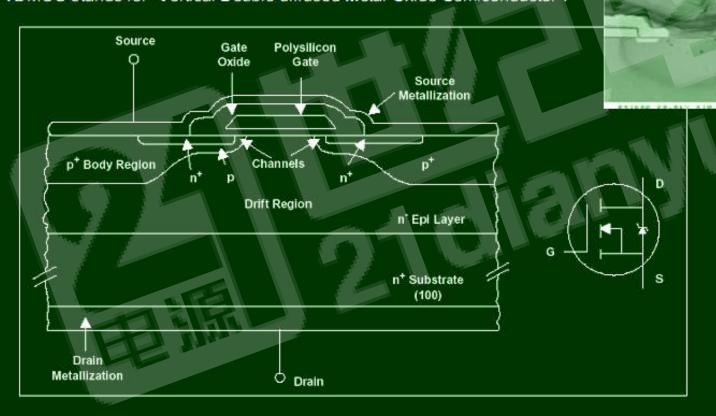


#### **VDMOS**

垂直导电-双扩散-金属-氧化层-半导体-场效晶体管

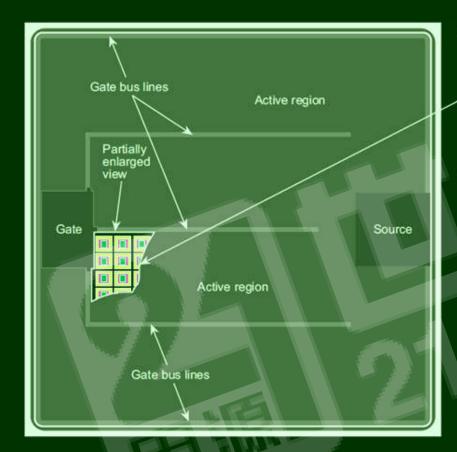
Vertical-Double diffused-Metal-Oxide-Semiconductor Field-Effect Transistor, VDMOSFET

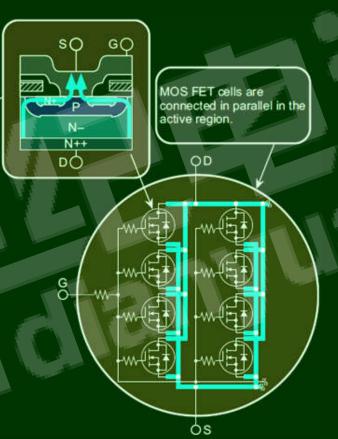
VDMOS stands for "Vertical Double diffused Metal Oxide Semiconductor".





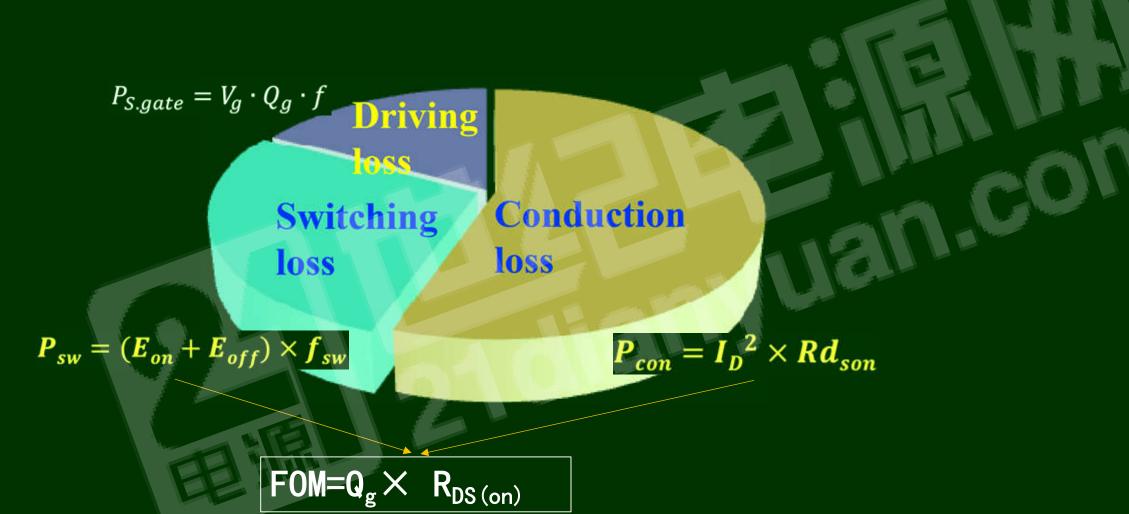
#### VD MOSFET芯片结构





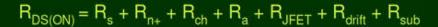


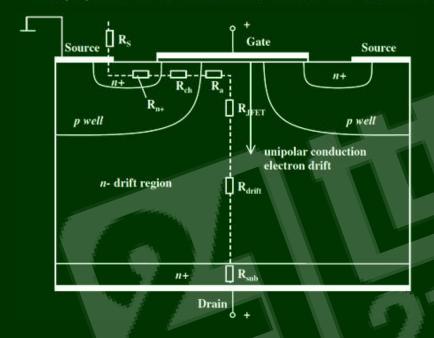
#### 功率MOSFET的相关损耗构成





#### 平面VD MOSFET剖面图 — 导通电阻





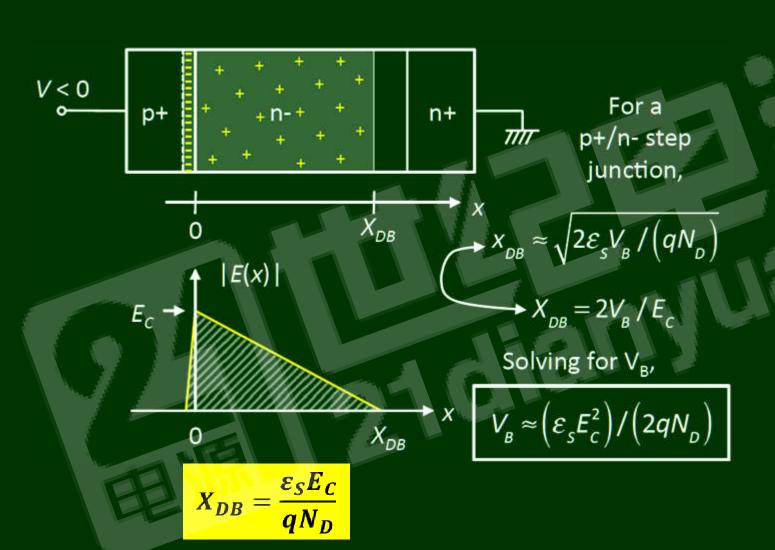
Planar	VD MOS	R <sub>DS (on)</sub>	构成及	分布
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R <sub>DS(on)</sub>								
V <sub>DS</sub> =30V	V <sub>DS</sub> =600V							
R <sub>S</sub> =7%	R <sub>s</sub> =0.5%							
R <sub>n+</sub> =6%	R <sub>n+</sub> =0.5%							
R <sub>ch</sub> =28%	R <sub>ch</sub> =1.5%							
R <sub>a</sub> =23%	R <sub>a</sub> =0.5%							
R* <sub>drift</sub> =29%	R* <sub>drift</sub> =96.5%							
R <sub>sub</sub> =7%	R <sub>sub</sub> =0.5%							
* R <sub>JFET</sub> is included in R <sub>drift</sub>								

不同电压等级平面MOSFET R<sub>dson</sub>分布

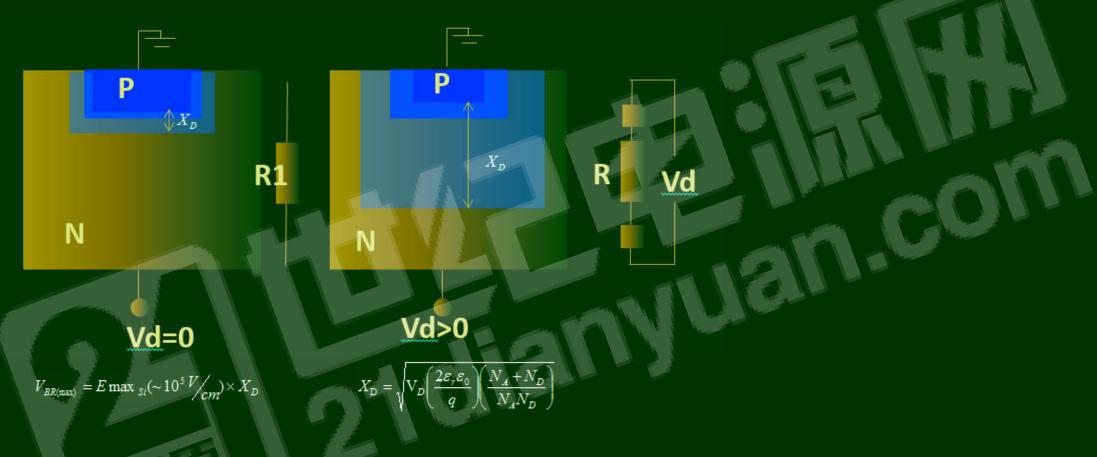


### 反向击穿情况下的PN结





#### 传统VDMOS PN结

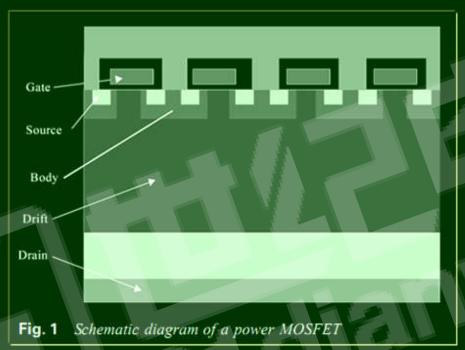


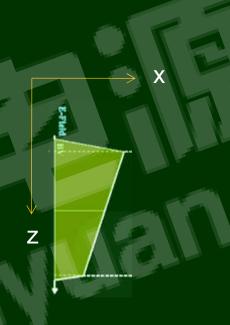
- 功率型MOSFET的耐压和PN结的反偏耗尽区宽度正比
- □ 耗尽区的宽度与P/N的浓度反比
- □ 电阻R与P/N的浓度成反比



#### 超结VDMOS技术路径——器件机理

#### 传统平面DMOS

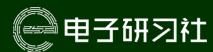




Electric field is one dimensional for conventional planar DMOS

$$\vec{E}(z) = \hat{z} \frac{q N_{\rm D}}{\varepsilon_{\rm s}} (W - z)$$

$$R_{\rm drift}^{\rm c} = \frac{2A^{1/2}}{\mu_{\rm n} \varepsilon_{\rm s}} B V^{2.5}$$



#### 超结功率VDMOS----重要专利

1. D. J Coe

D. J. Coe. High Voltage Semiconductor Device, U. S. Patent 4,754,310, 1988.



2. X. B. Chen

X. B. Chen. Semiconductor Power Devices with Alternating Conductivity Type High-voltage Breakdown Regions.

U. S. Patent 5,216,275, 1993.





3. J. Tibanyi

J. Tihanyi. Power MOSFET, U. S. Patent 5, 438, 215, 1995. 1998年超结MOS 开始商用!

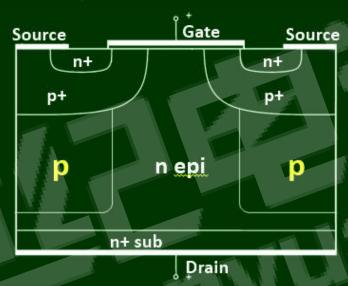


#### 传统VD MOS 和SJ MOS的剖面图对比

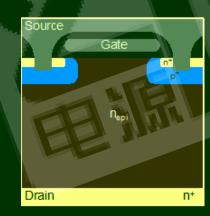
#### 传统VD MOSFET



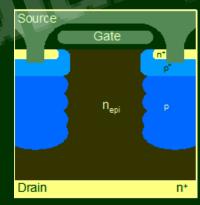
#### Super Junction MOSFET

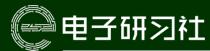


#### **Standard MOSFET**

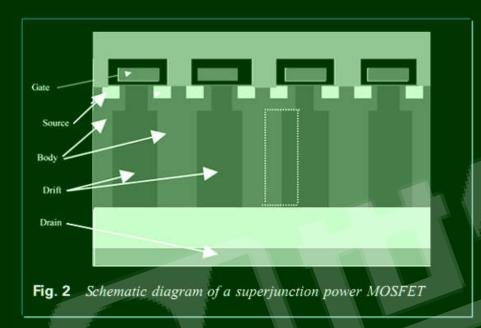


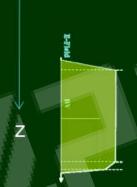
#### SJ MOSFET





#### 超结VDMOS技术路径——器件机理





超结DMOS

N pillar doping is typically 1 order higher than that of conventional planar DMOS, accordingly superjunction MOSFET R on spreduces significantly.

Electric field is two dimensional far from device edge for superjunction DMOS

$$\vec{E}(x, z) = \hat{z} \frac{V_{\rm D}}{W} + \hat{x} \frac{2qN_{\rm D}}{\varepsilon_{\rm s}} \left( x - \frac{x_{\rm n}}{2} \right)$$

N region

$$\vec{E}(x, z) = \hat{z} \frac{V_{\rm D}}{W} - \hat{x} \frac{2qN_{\rm A}}{\varepsilon_{\rm s}} \left( x + \frac{x_{\rm p}}{2} \right)$$

P region

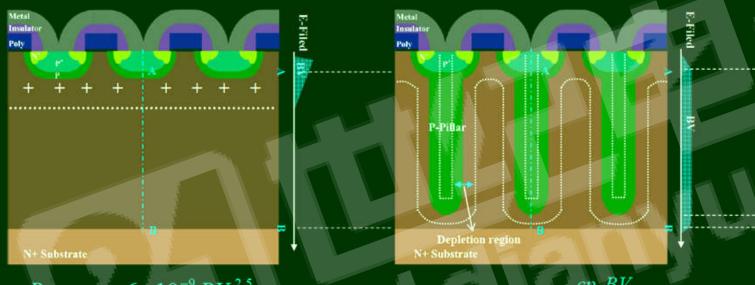
$$R_{\text{drift}}^{\text{s}} = \frac{W_{\text{c}}}{q\mu_{\text{n}}N_{\text{D}}} = \frac{2A^{1/6}x_{\text{n}}BV^{7/6}}{\mu_{\text{n}}\varepsilon_{\text{s}}E_{\text{L}}^{\text{c}}}$$



### 内部电场对比1







$$Ron, sp = 6 \times 10^{-9} BV^{2.5}$$

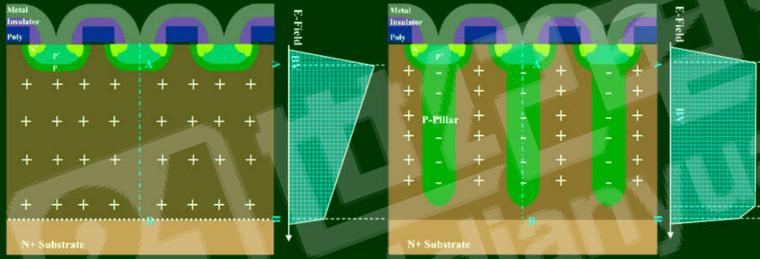
$$Ron, sp = \frac{cp.BV}{2q\mu E \cdot Q}$$

普通PN结和超级结电场分布

### 内部电场对比3

• Planar MOSFET

• Super-Junction MOSFET



Area is proportional to BV

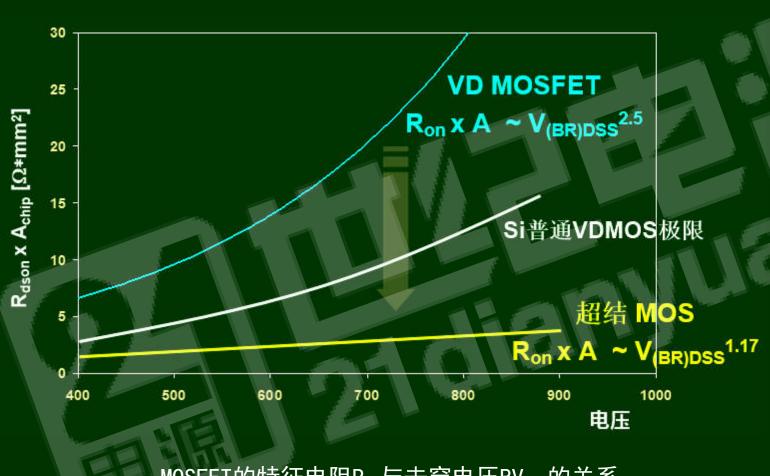
Area is twice so BV is twice for same doping thanks to charge balance

· Si limitation: On resistance and BV is trade-off

· On resistance is in linear relation on BV



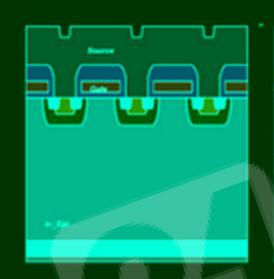
## 特征导通电阻Rsp(=R<sub>(ds)on</sub>\*A<sub>chip</sub>)对比

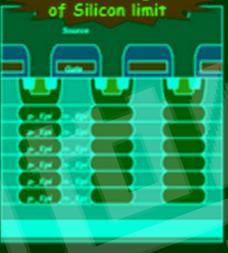


MOSFET的特征电阻R<sub>sp</sub>与击穿电压BV<sub>DSS</sub>的关系



#### 制造工艺示意图 (普通VDMOS VS. 超结MOS)





Break through



普通平面VDMOS

超结MOS 多次外延工艺

超结MOS 深沟槽工艺

#### Split-gate MOSFET 分立栅MOSFET

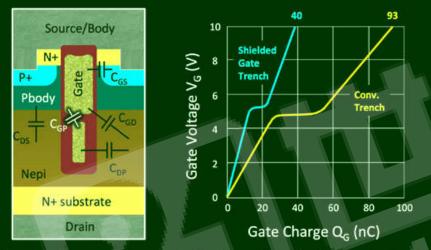


Fig. 9. Cross section and gate charge benefit of split-gate trench VDMOS.



Specific on-resistance of Split-Gate MOSFET against breakdown voltage



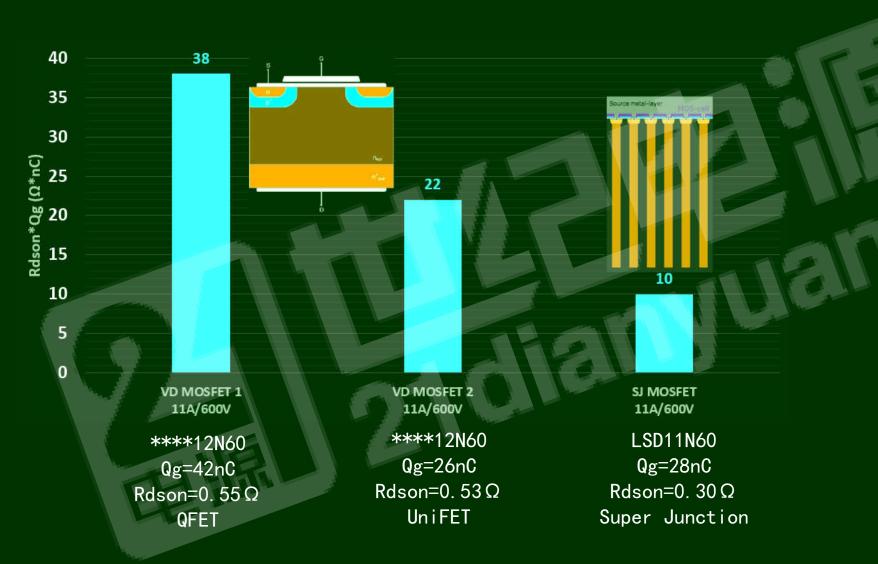
# 芯片面积对比(600V/11A)

VDMOS	SJ MOSFET								
VDINIOS	GEN 1	GEN 2	GEN 3						
Die Size: $21.6 \text{ mm}^2$ $R_{DSon}$ : $0.65 \Omega$	Die Size: 12 mm² R <sub>DSon</sub> : 0.35 Ω	Die Size: 8.6 mm² R <sub>DSon</sub> : 0.38 Ω	Die Size: ~5.6 mm² R <sub>DSon</sub> : 0.38 Ω						





# FOM (=Qg\*RDS(on)) 对比(VDMOS Vs. SJ MOS)



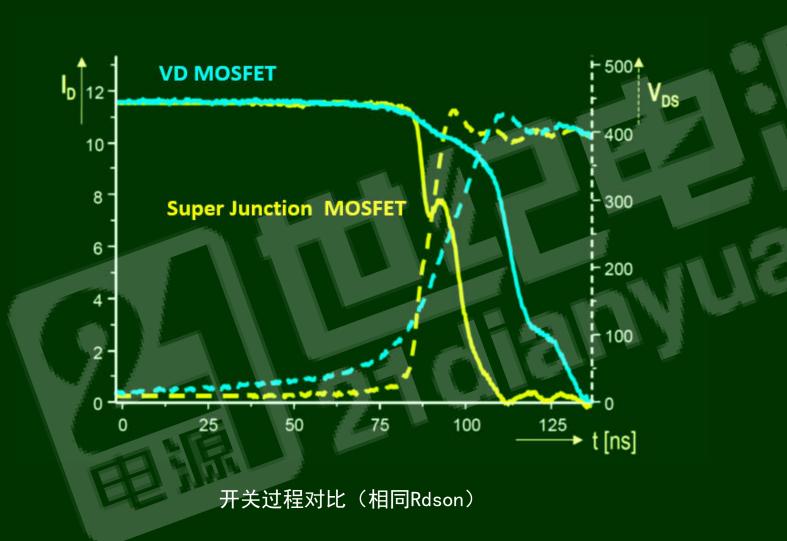


# FOM(=Qg\*RDS(on)) 对比(SJ MOS Vs. GaN HEMTs)





#### 超结MOSFET和普通平面MOSFET开关特性对比





## 器件关键参数对比

测试项目	1) VGSTH	2)RDSON 导通电阻	3)BVDSS 击穿电压	4)Qg 栅极电荷	5)IAS 雪崩电流	备注
	[ V ]	[Ω]	[ V ]	[ nC ]	[ A ]	
测试条件	ID = 250.1UA	VGS = 10.01 V	ID = 250.1UA	VGS=10V	VGS=10V	
		ID = 2.000 A	40	ID=2A (SJ) / ID=4A (P)	L=500uH	
LSX65R930GT	4. 0	0. 80	718	13. 6	6. 5	超级结L3
LSX65R950HT	3. 6	0. 86	680	7. 6	9.5	超级结L4
LND4N65	2.8	2. 3	706	11.6	13	高压平面
SVF4N65	2. 9	2. 5	705	11.1	15	高压平面



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#### MOSFET规格书解读-极限值

## **2 Maximum ratings** at $T_j = 25^{\circ}\text{C}$ , unless otherwise specified

Maximum ratings Table 2

Baramatar	Cumbal		Value	S	Linia	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Continuous drain current <sup>1)</sup>	10			23.8 15.0	A	Tc=25°C Tc=100°C
Pulsed drain current <sup>2)</sup>	/D,pulse	-	-	68	A	Tc=25°C
Avalanche energy, single pulse	E <sub>AS</sub>	-	A \	497	mJ	I <sub>D</sub> =4.1A; V <sub>DD</sub> =50V; see table 12
Avalanche energy, repetitive	<b>E</b> AR	-		0.75	mJ	I <sub>D</sub> =4.1A; V <sub>DD</sub> =50V; see table 12
Avalanche current, repetitive	I <sub>AR</sub>			4.1	Α	
MOSFET dv/dt ruggedness	dv/dt	43	•	100	V/ns	V <sub>DS</sub> =0400V
Gate source voltage (static)	V <sub>G</sub> s	-20		20	V	static;



### 规格书解读一极限值

Barrana	Combal	Values			Ilmia		
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition	
Power dissipation (Non FullPAK) TO-220, TO-263, TO-247	P <sub>tot</sub>	-	-	176	w	T <sub>C</sub> =25°C	
Power dissipation (FullPAK) TO-220FP	P <sub>tot</sub>	-	-	34	W	Tc=25°C	
Storage temperature	T <sub>stg</sub>	-55		150	°C	-	
Operating junction temperature	T <sub>j</sub>	-55	- 1	150	°C		
Mounting torque (Non FullPAK) TO-220, TO-247		-		60	Ncm	M3 and M3.5 screws	
Mounting torque (FullPAK) TO-220FP	+11	-		50	Ncm	M2.5 screws	
Continuous diode forward current	Is	-		20.6	A	Tc=25°C	
Diode pulse current <sup>2)</sup>	/s,pulse			68	A	Tc=25°C	
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	A	15	V/ns	$V_{\rm DS}$ =0400V, $I_{\rm SD}$ <= $I_{\rm S}$ , $T_{\rm j}$ =25°C see table 10	
Maximum diode commutation speed	di <sub>f</sub> /dt			500	A/μs	$V_{\rm DS}$ =0400V, $I_{\rm SD}$ <= $I_{\rm S}$ , $T_{\rm j}$ =25°C see table 10	
Insulation withstand voltage for TO-220FP	V <sub>ISO</sub>			2500	V	V <sub>rms</sub> , T <sub>C</sub> =25°C, <i>t</i> =1min	





#### 规格书解读-热阻

Table 4 Thermal characteristics (FullPAK) TO-220FP

Baramatar	Cumbal	Values			Unit	Note / Test Condition	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition	
Thermal resistance, junction - case	RthJC	2	-	3.67	°C/W		
Thermal resistance, junction - ambient	R <sub>thJA</sub>	-		80	°C/W	leaded	
Soldering temperature, wavesoldering only allowed at leads	T <sub>sold</sub>			260	°C	1.6mm (0.063 in.) from case for 10s	





### 规格书解读一静态参数

Table 6 Static characteristics

Barrana	Combal		Values				
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition	
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	600		-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =1mA	
Gate threshold voltage	V <sub>(GS)th</sub>	3.5	4.0	4.5	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =0.75mA	
Zero gate voltage drain current	I <sub>DSS</sub>	1	10	1	μА	V <sub>DS</sub> =600, V <sub>GS</sub> =0V, T <sub>j</sub> =25°C V <sub>DS</sub> =600, V <sub>GS</sub> =0V, T <sub>j</sub> =150°C	
Gate-source leakage current	/ <sub>GSS</sub>		*	100	nA	V <sub>GS</sub> =20V, V <sub>DS</sub> =0V	
Drain-source on-state resistance	R <sub>DS(on)</sub>		0.144 0.374	0.160	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =9A, T <sub>j</sub> =25°C V <sub>GS</sub> =10V, I <sub>D</sub> =9A, T <sub>j</sub> =150°C	
Gate resistance	R <sub>G</sub>		1.6		Ω	f=1MHz, open drain	



### 规格书解读-动态参数

Table 7 Dynamic characteristics

Baranata	Cumbal		Values		11	Note / Test Condition
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Input capacitance	Ciss	-	2080	- 1	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz
Output capacitance	Coss		89		pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz
Effective output capacitance, energy related <sup>1)</sup>	C <sub>o(er)</sub>	-	72		pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =0400V
Effective output capacitance, time related <sup>2)</sup>	C <sub>o(tr)</sub>	-	313		pF	/ <sub>D</sub> =constant, V <sub>GS</sub> =0V, V <sub>DS</sub> =0400V





## 规格书解读-栅极电荷

Table 8 Gate charge characteristics

	0		Value	S			
Parameter	Symbol	Min.	Тур. Мах.		Unit	Note / Test Condition	
Gate to source charge	Q <sub>gs</sub>		13	# 1	nC	V <sub>DD</sub> =400V, I <sub>D</sub> =11.3A, V <sub>GS</sub> =0 to 10V	
Gate to drain charge	Q <sub>gd</sub>		15	-	nC	V <sub>DD</sub> =400V, I <sub>D</sub> =11.3A, V <sub>GS</sub> =0 to 10V	
Gate charge total	Qg	-	44		nC	V <sub>DD</sub> =400V, I <sub>D</sub> =11.3A, V <sub>GS</sub> =0 to 10V	
Gate plateau voltage	V <sub>plateau</sub>	-	6.1	-\	V	V <sub>DD</sub> =400V, I <sub>D</sub> =11.3A, V <sub>GS</sub> =0 to 10V	





### 规格书解读-体二极管

Table 9 Reverse diode characteristics

Barrana	Cumbal		Values	S	Harris	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Diode forward voltage	V <sub>SD</sub>		0.9	# \	V	V <sub>GS</sub> =0V, I <sub>F</sub> =11.3A, T <sub>j</sub> =25°C
Reverse recovery time	t <sub>rr</sub>	-	350		ns	V <sub>R</sub> =400V, I <sub>F</sub> =11.3A, d <i>i</i> <sub>F</sub> /d <i>t</i> =100A/μs; see table 10
Reverse recovery charge	Q <sub>rr</sub>		5.3		μC	V <sub>R</sub> =400V, I <sub>F</sub> =11.3A, d <i>i</i> <sub>F</sub> /d <i>t</i> =100A/μs; see table 10
Peak reverse recovery current	I <sub>rrm</sub>		28		A	V <sub>R</sub> =400V, J <sub>F</sub> =11.3A, d <i>i</i> <sub>F</sub> /d <i>t</i> =100A/μs; see table 10





#### GS和DS击穿电压

Vgs: 栅极(G)与源极(S)之间所能施加的最大电压值。

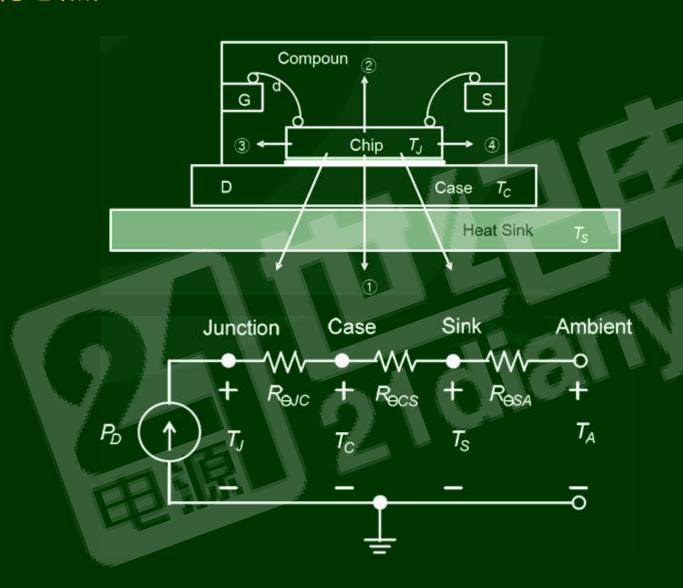


Voss:漏极(D)与源极(S)之间所能施加的最大电压值。



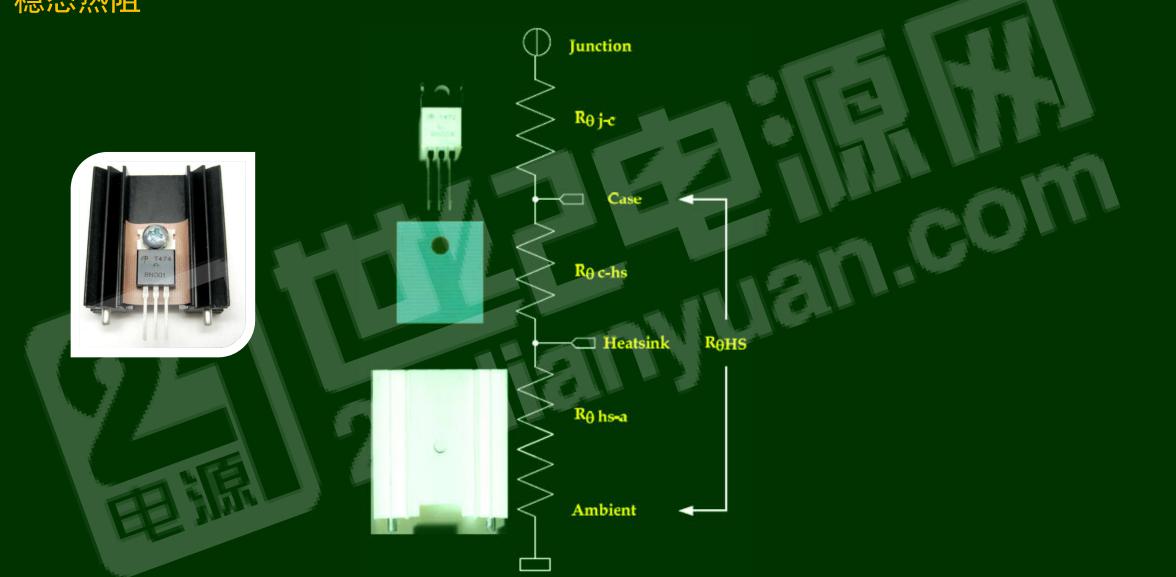


#### 稳态热阻



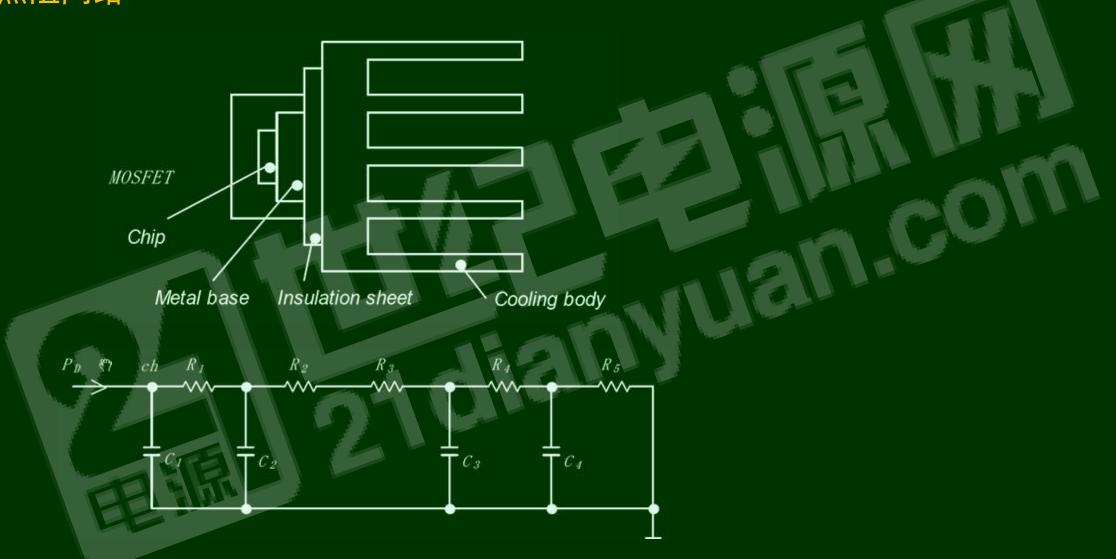


#### 稳态热阻





#### 热阻网络

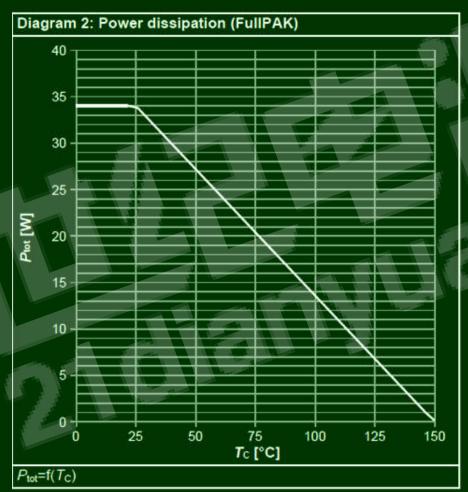




#### 耗散功率PD和连续漏极电流ID



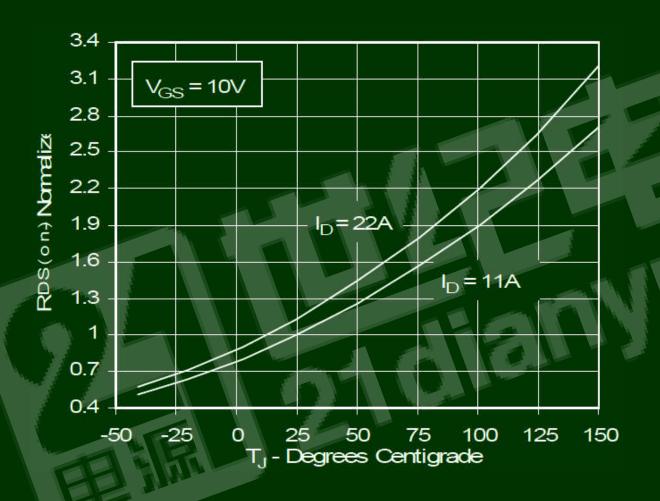
$$P_D = \frac{T_{J(\text{max})} - T_a}{R_{\Theta J(\text{max})}}$$







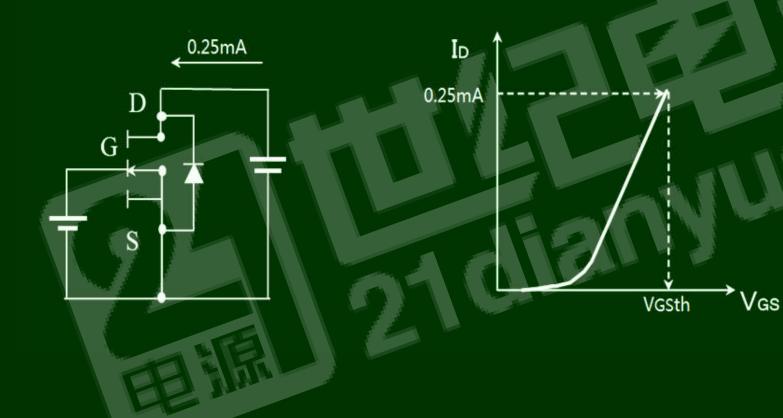
#### 导通电阻Rdson





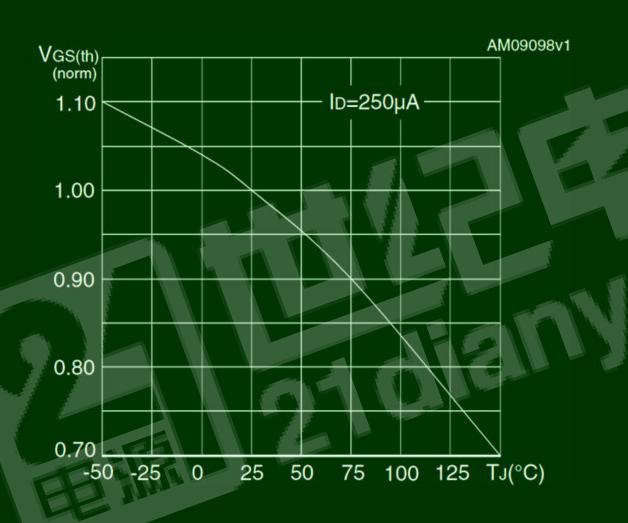
#### 栅极阈值电压VGS(th)

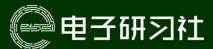
MOSFET的VDS=VGS, ID = 0.25mA时的栅极电压VGS



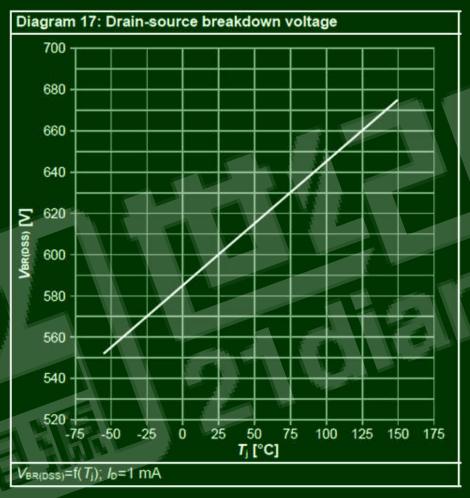


#### 栅极阈值电压VGS(th)随温度变化





#### 击穿电压BV随温度变化



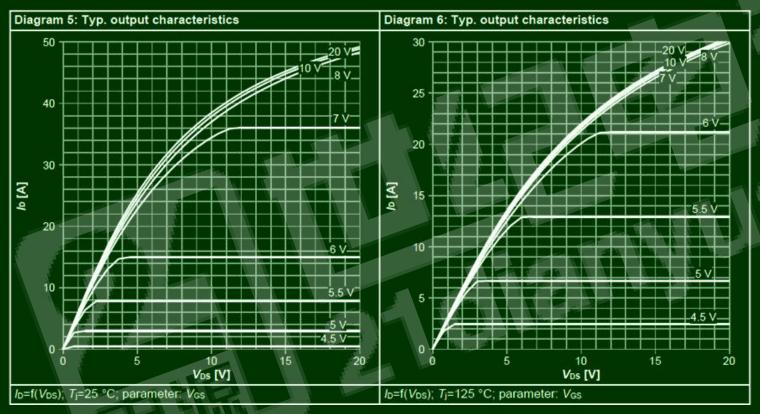




# MOSFET脉冲电流的测试波形 $\mathsf{I}_{\mathsf{DM}}$ Tw



#### MOSFET输出特性曲线





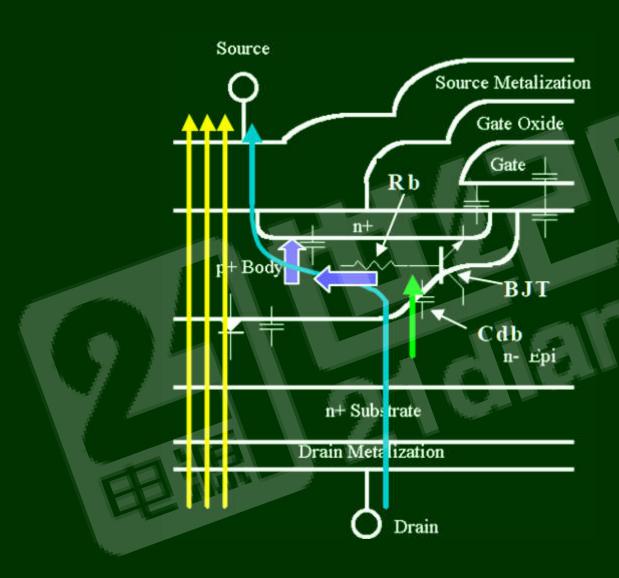


#### 关于脉冲电流的限制因素

- •限制条件1: MOSFET的结温,在比较大的脉冲电流情况下,在一定的驱动电压情况下,MOSFET的压降相对较大,MOSFET的瞬间功耗比较大,导致MOSFET的结温会快速升高。保证不超过MOSFET的150度结温的限制,决定了脉冲电流的大小。
- •限制条件2: MOSFET键合线。在比较大的脉冲电流情况下, MOSFET的源极键合线(Bonding线)的瞬态功耗也会增加,导致其 温度也会升高,由于塑封料包裹着键合线。如果键合线的温度超 过220度,会使得塑封材料发生化学分解,进而导致封装失效。这 也决定了脉冲电流的大小。
- •以上限制条件1和限制条件2的最小值决定了器件的最大脉冲电流。

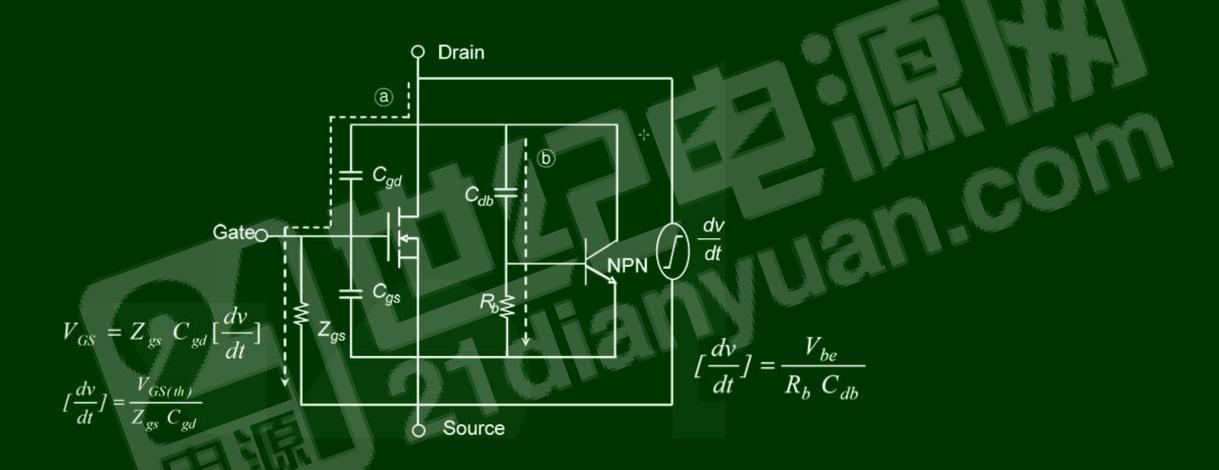


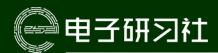
#### MOSFET内部结构图(位移电流、反向恢复电流、雪崩电流)





#### MOSFET dv/dt能力



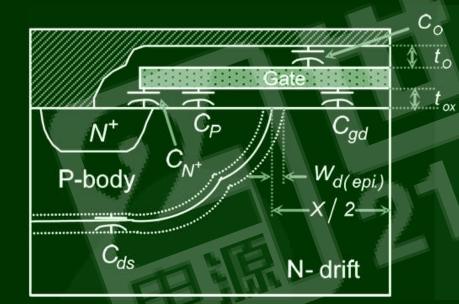


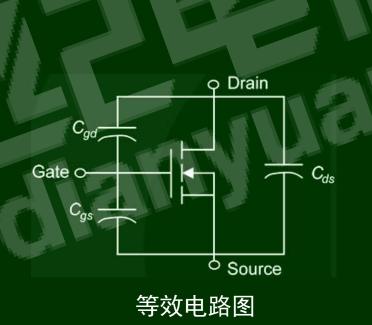
#### MOSFET结电容

输入电容:  $C_{iss} = C_{gd} + C_{gs}$ 

输出电容:  $C_{oss} = C_{gd} + C_{ds}$ 

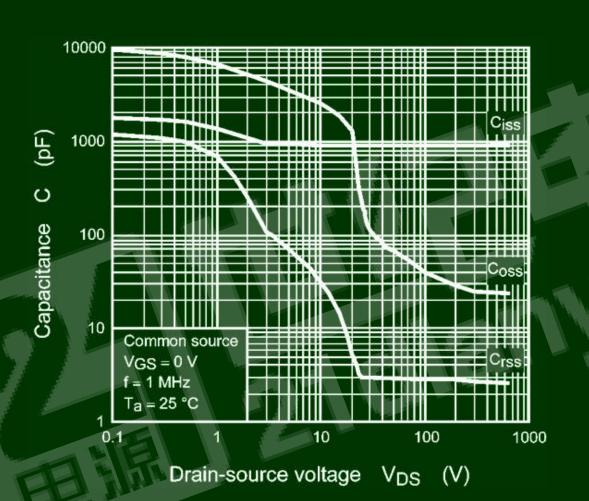
米勒电容: C<sub>rss</sub> = Cgd

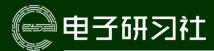




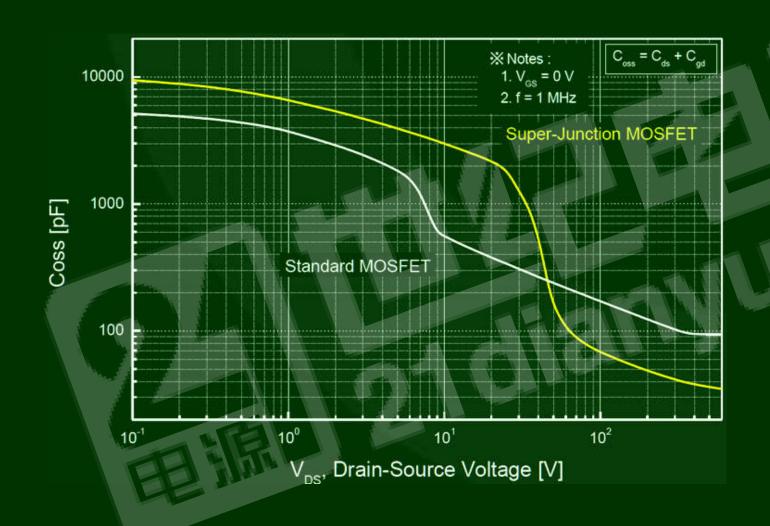


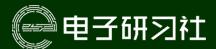
#### MOSFET结电容随VDS变化规律



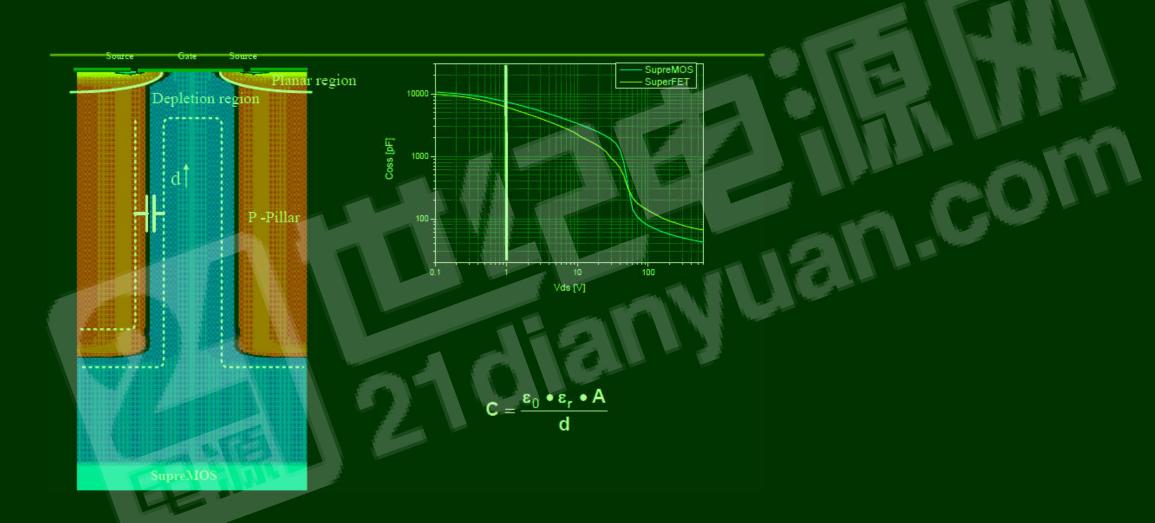


#### MOSFET结电容变化对比



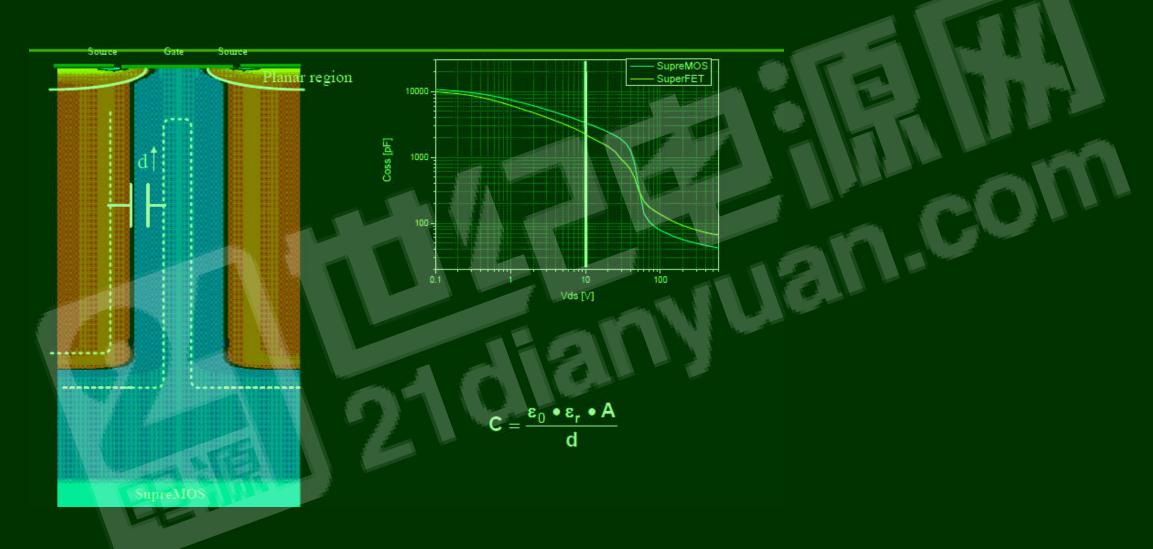


#### 超结MOSFET结电容随Vds变化规律



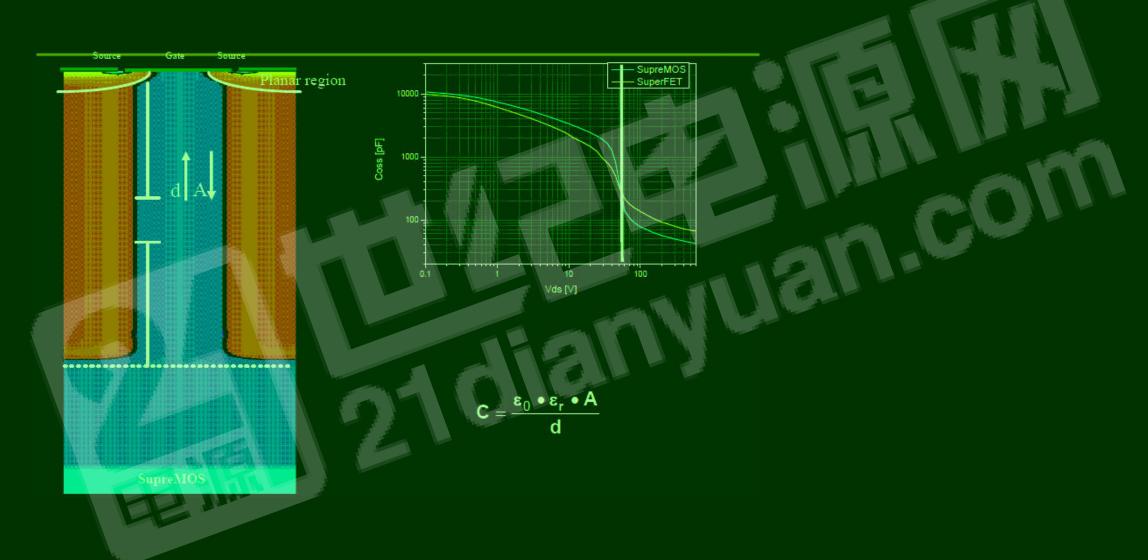


#### 超结MOSFET结电容随Vds变化规律





#### 超结MOSFET结电容随Vds变化规律





#### 如何得到MOSFET的Ceq?

#### Dynamic characteristics

Input capacitanco	C iss	V <sub>GS</sub> =0 V, V <sub>DS</sub> =100 V,	70	2800
Output capacitance	C oss	f=1 MHz		130
Effective output capacitance, energy related <sup>5)</sup>	C o(er)	$C_{eq} = C_{o(tr)}$ $V_{GS} = 0 \ \forall . \ V_{DS} = 0 \ \forall$	1	130
Effective output capacitance, time related <sup>6)</sup>	C o(tr)	to 480 V		340

$$\begin{cases} Q_{\text{eq}} = C_{o(tr)} \cdot V \\ Q_{\text{eq}} = \int_{0}^{Vds} C(v) \, dv \end{cases}$$

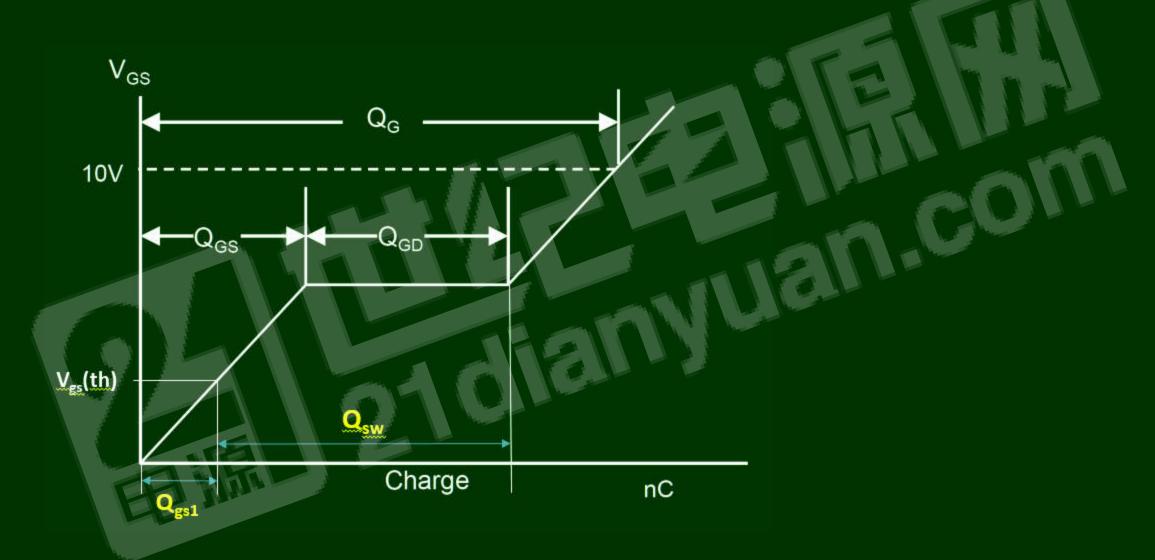
$$\begin{cases} E_{\text{eq}} = \frac{1}{2} \cdot C_{o(er)} \cdot V^2 \\ E_{\text{eq}} = \int_0^{Vds} C(v) v \, dv \end{cases}$$

<sup>&</sup>lt;sup>5)</sup>  $C_{\text{o(er)}}$  is a fixed capacitance that gives the same stored energy as  $C_{\text{oss}}$  while  $V_{\text{DS}}$  is rising from 0 to 80%  $V_{\text{DSS}}$ .

<sup>&</sup>lt;sup>6)</sup>  $C_{\text{o(tr)}}$  is a fixed capacitance that gives the same charging time as  $C_{\text{oss}}$  while  $V_{\text{DS}}$  is rising from 0 to 80%  $V_{\text{DSS}}$ .

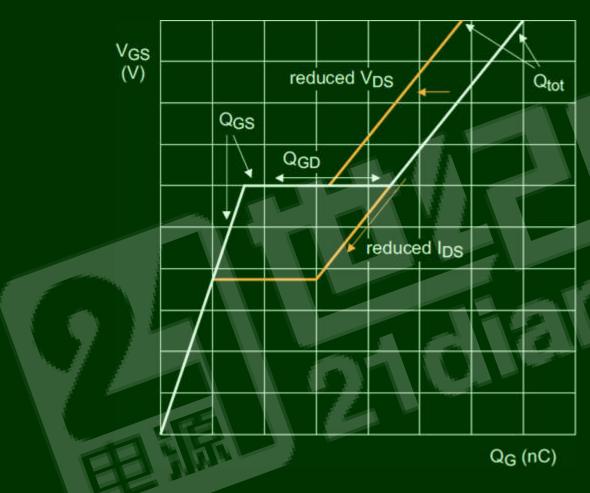


#### MOSFET栅极电荷Qg





#### 不同因素对Qg曲线的影响





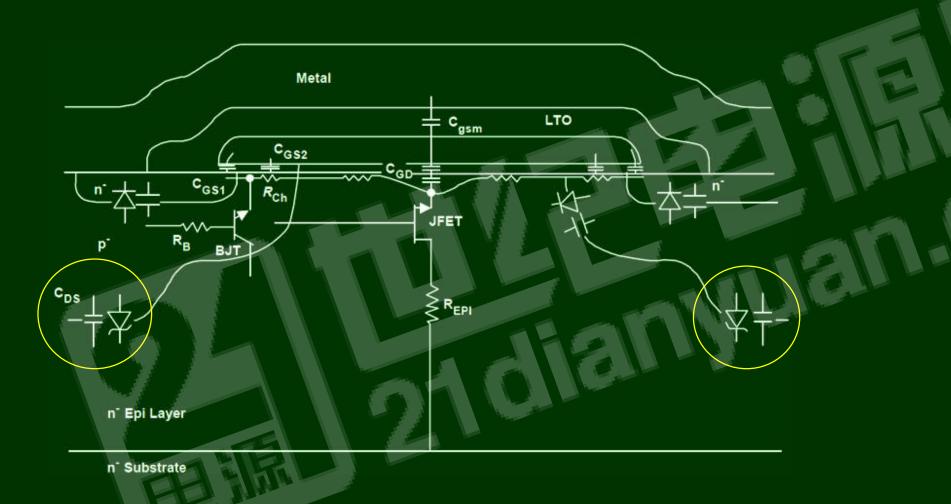


#### 安全工作区SOA



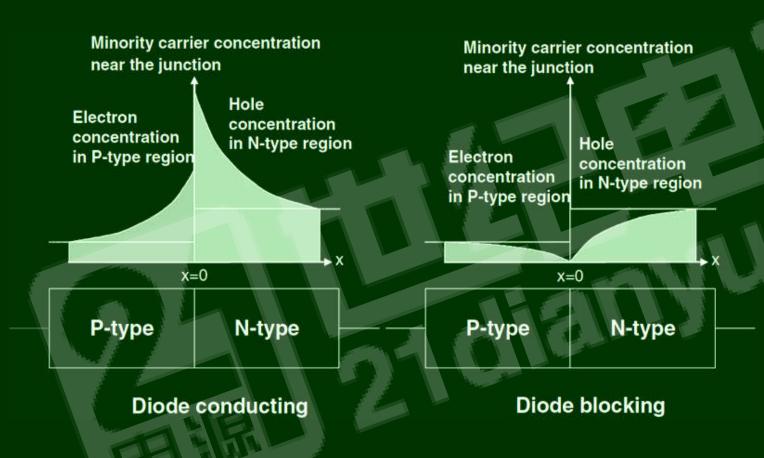


#### 体二极管



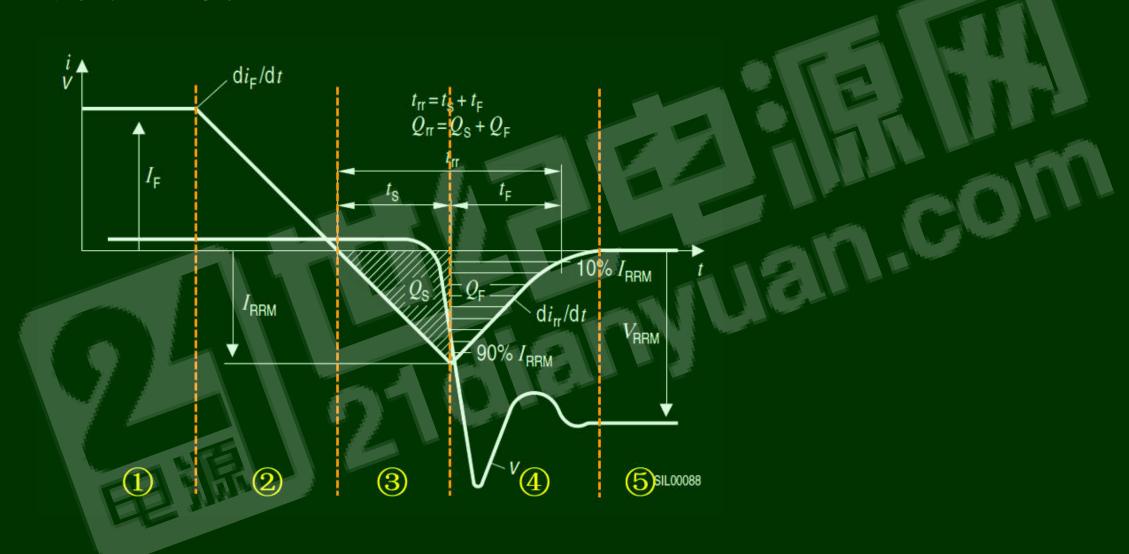


#### 二极管导通和反偏状态





#### 二极管反向恢复曲线



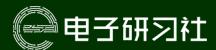


#### 体二极管主要参数

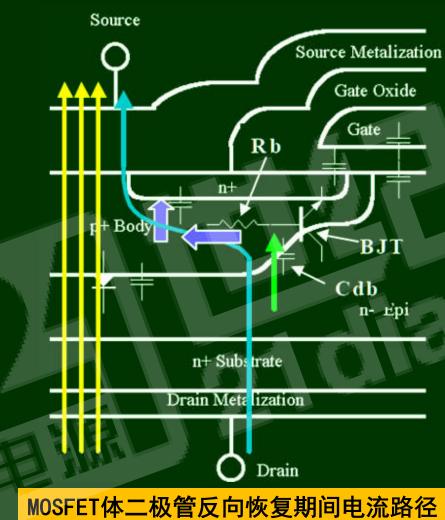
Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	
		Min.	Typ. Max.				
Diode forward voltage	$V_{\mathrm{SD}}$		0.9		V	$V_{\rm GS}$ =0 V, $I_{\rm F}$ =11 A, $T_{\rm j}$ =25 °C	
Reverse recovery time	<i>I</i> m	+	410	-	ns	V <sub>R</sub> =400 V, I <sub>F</sub> =11 A,	
Reverse recovery charge	$Q_{\rm rr}$	-	6.1	- 1	μC	d <i>i</i> <sub>F</sub> /d <i>t</i> =100 A/μs	
Peak reverse recovery current	$I_{ m rm}$	-	28	•	Α	MI PA	



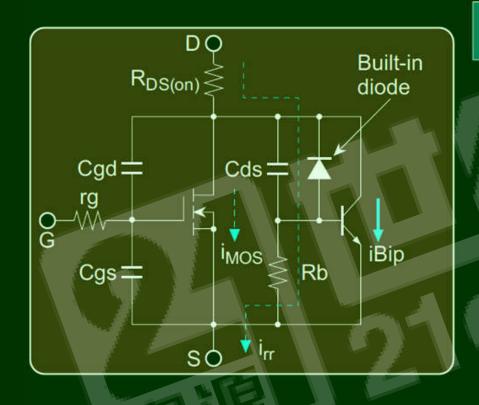


## MOSFET体二极管反向恢复电流路径 (位移电流、反向恢复电流、雪崩电流)

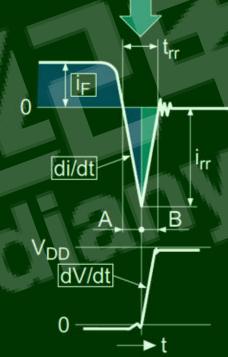




#### 体二极管dv/dt能力及反向恢复导致的失效机理

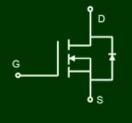


Destruction occurs while the diode voltage is recovering.





#### MOSFET雪崩能力



### 雪崩能力

- 电压浪涌测试Surge
- 输入电压突变
- 电源启动及短路

雪崩电流 I<sub>AS</sub>,I<sub>AR</sub>

寄生BJT导通,MOSFET 趋于开通。

雪崩能量 E<sub>AS</sub>,E<sub>AR</sub>

MOSFET局部元胞过热损 坏。



#### MOSFET雪崩能力

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		VDSS	650	V	
Gate-source voltage		Vgss	±30	V	
Drain current	DC (Note 1)	ID	13	1	
	Pulse (Note 1)	IDP	26		
Drain power dissipation (Tc = 25°C)		P <sub>D</sub>	40	W	
Single pulse avalanche energy (Note 2)		E <sub>AS</sub>	86	mJ	
Avalanche current		I <sub>AR</sub>	13	А	
Repetitive avalanche energy (Note 3)		E <sub>AR</sub>	4.0	mJ	

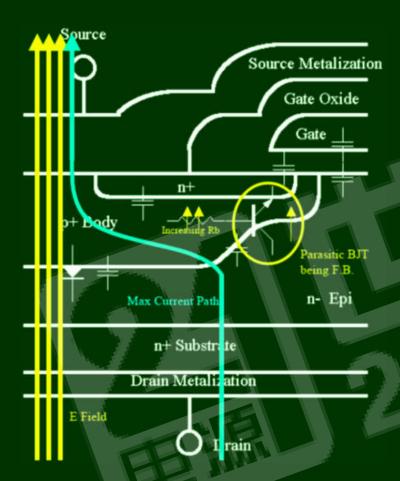
Note 2:  $V_{DD}$  = 90 V,  $T_{ch}$  = 25 °C (initial), L = 0.9 mH,  $R_G$  = 25  $\Omega$ ,  $I_{AR}$  = 13 A

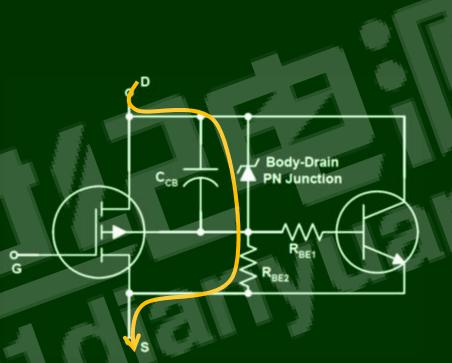
Note 3: Repetitive rating: pulse width limited by maximum channel temperature

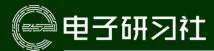




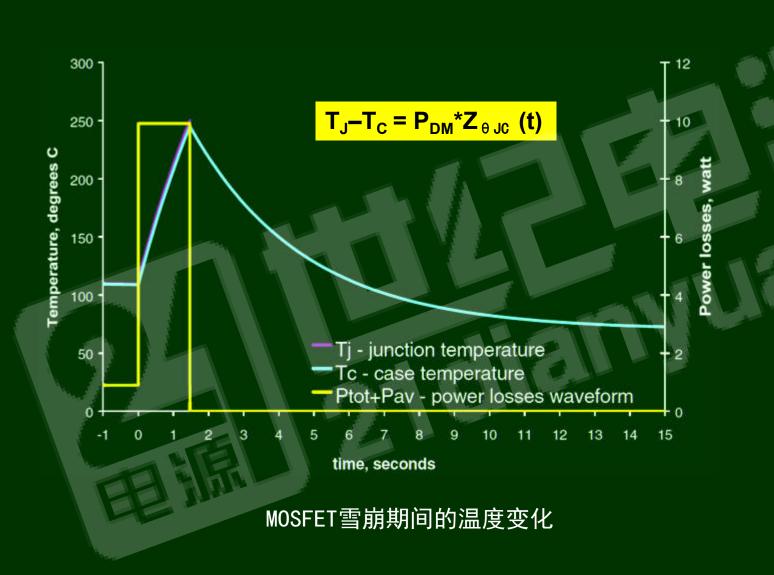
#### MOSFET雪崩电流路径及影响





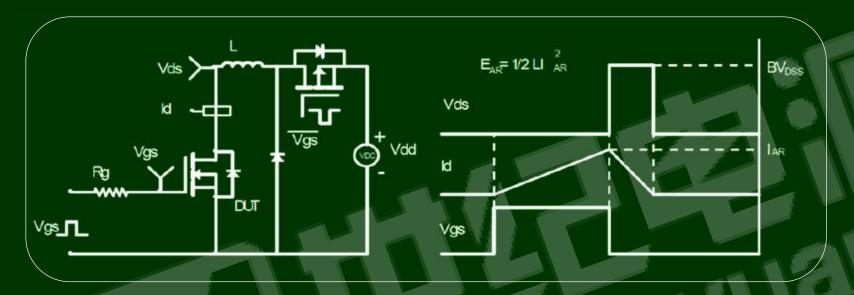


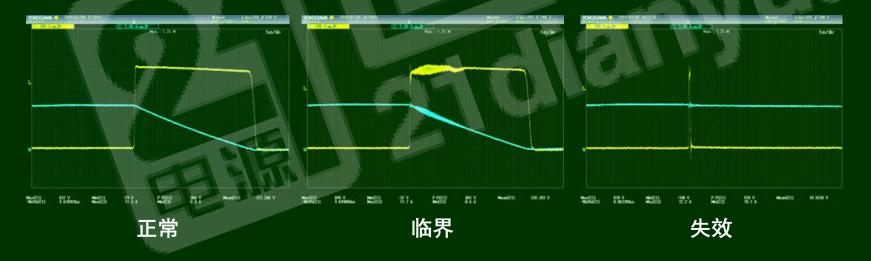
#### MOSFET雪崩特性

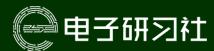




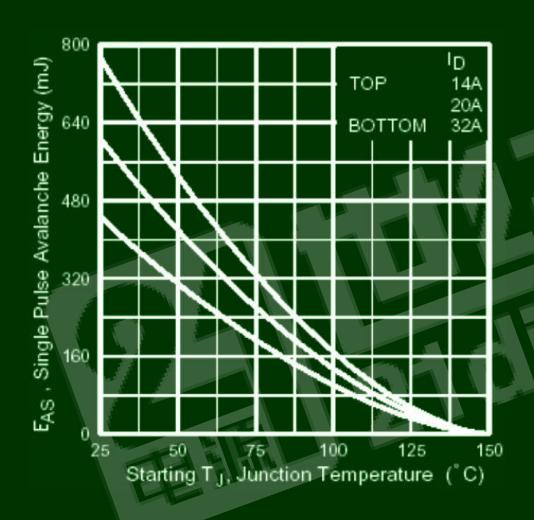
#### 雪崩能力测试电路







#### 雪崩能量 和 初始结温以及电流的关系



雪崩电流的变化使得 雪崩时间变化,从而 导致瞬态热阻的变化, 所以不同雪崩电流测 试条件下会得到不同 的雪崩能量大小。



## 主要内容

• 功率MOSFET的原理

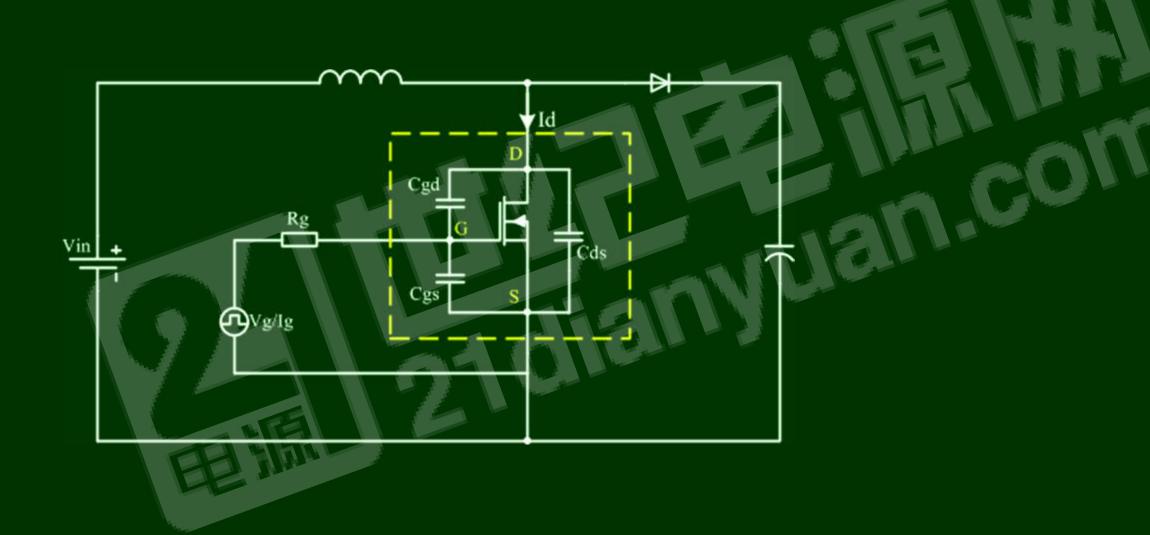
• 功率MOSFET的参数和特性

• 功率MOSFET的开关过程分析

• 功率MOSFET的典型应用分析

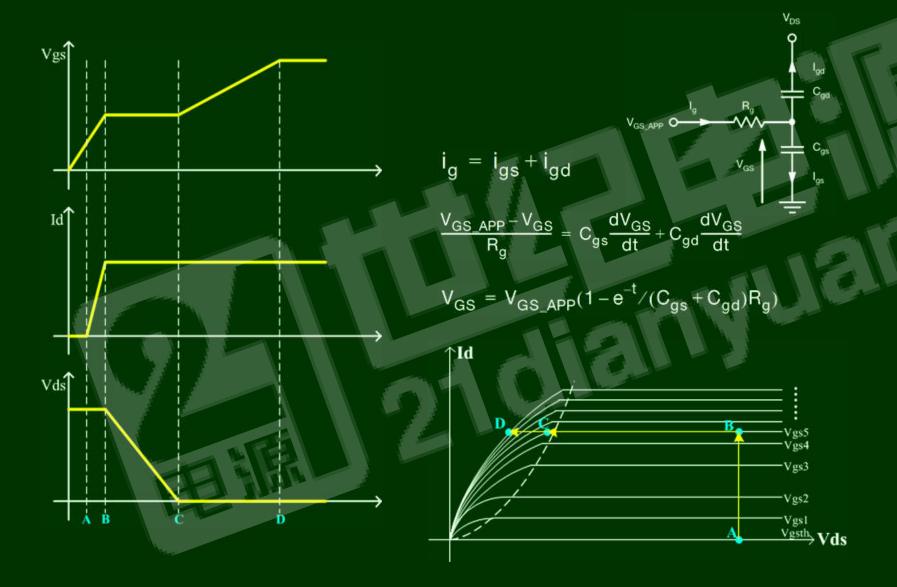


#### MOSFET在电路中的端口模型





#### 理想状态下开通过程-感性条件下



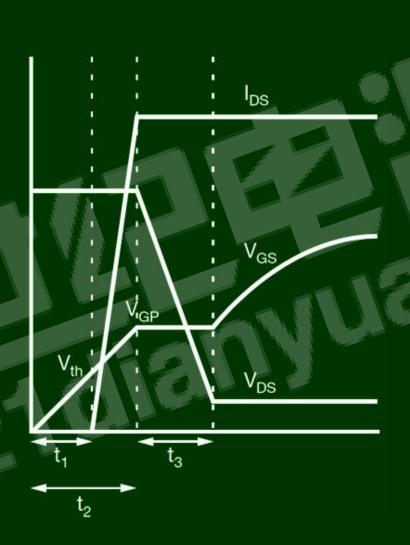


#### 开通过程的定量关系

$$t_1 = (R_g + R_{g\_app})(C_{gs} + C_{gd}) ln \left(\frac{1}{1 - \frac{V_{th}}{V_{GS\_APP}}}\right)$$

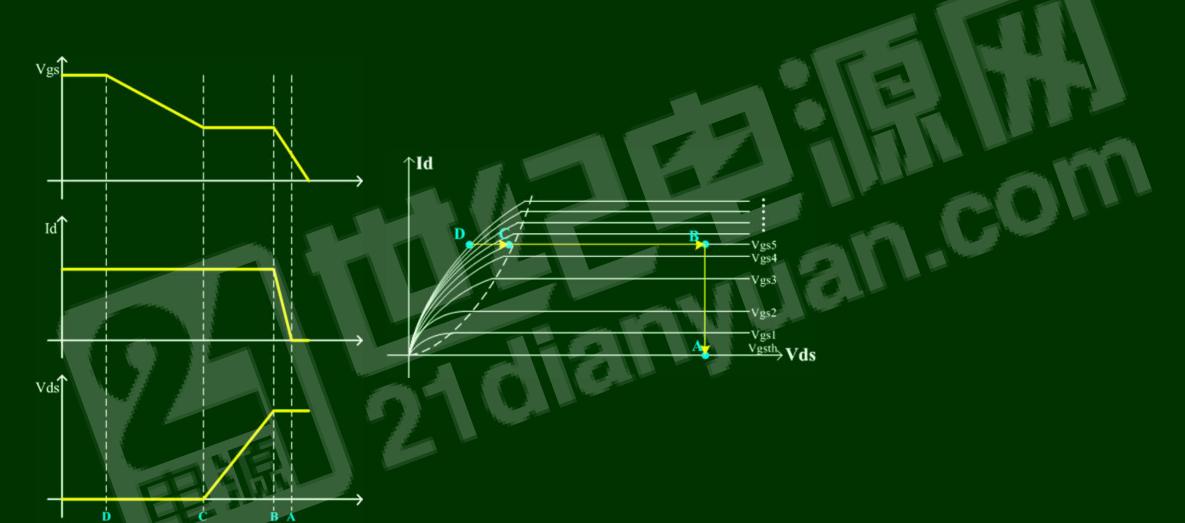
$$t_2 = (R_g + R_{g\_app})(C_{gs} + C_{gd}) \ln \left( \frac{1}{1 - \frac{V_{GP}}{V_{GS\_APP}}} \right)$$

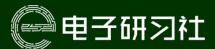
$$t_3 = \frac{(V_{DS} - V_F)(R_g + R_{g\_app})C_{gd}}{V_{GS\_APP} - V_{GP}}$$



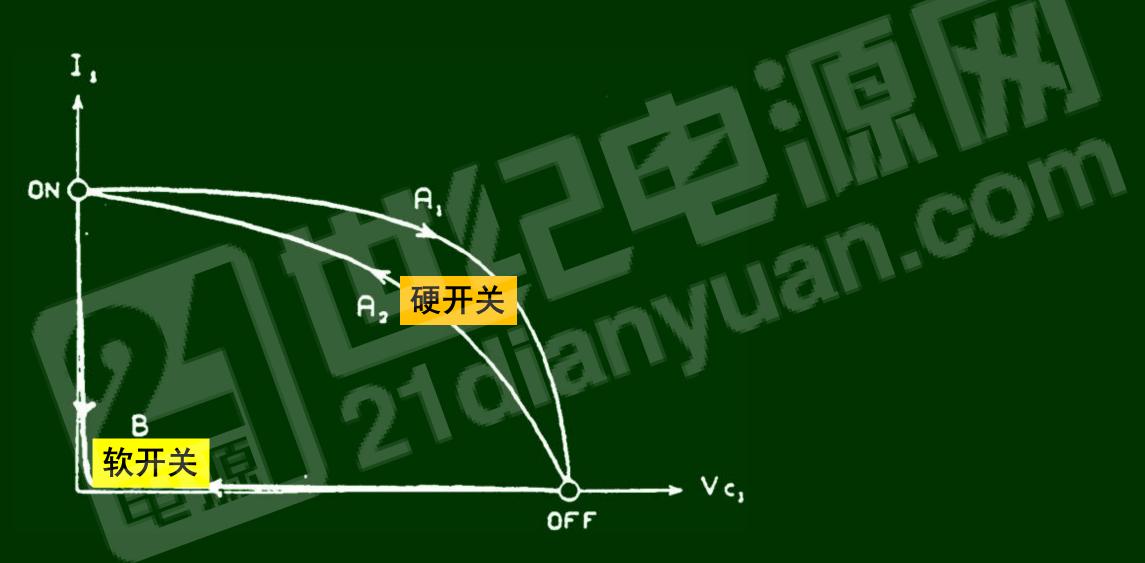


# 理想状态下关断过程-感性条件下



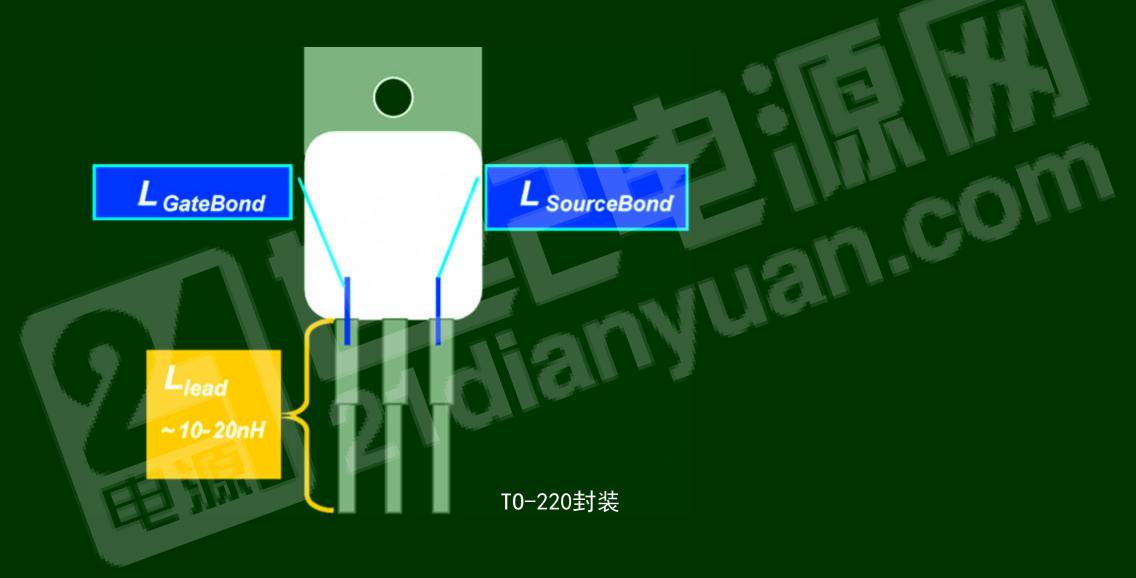


# 硬开关和软开关的I-V轨迹



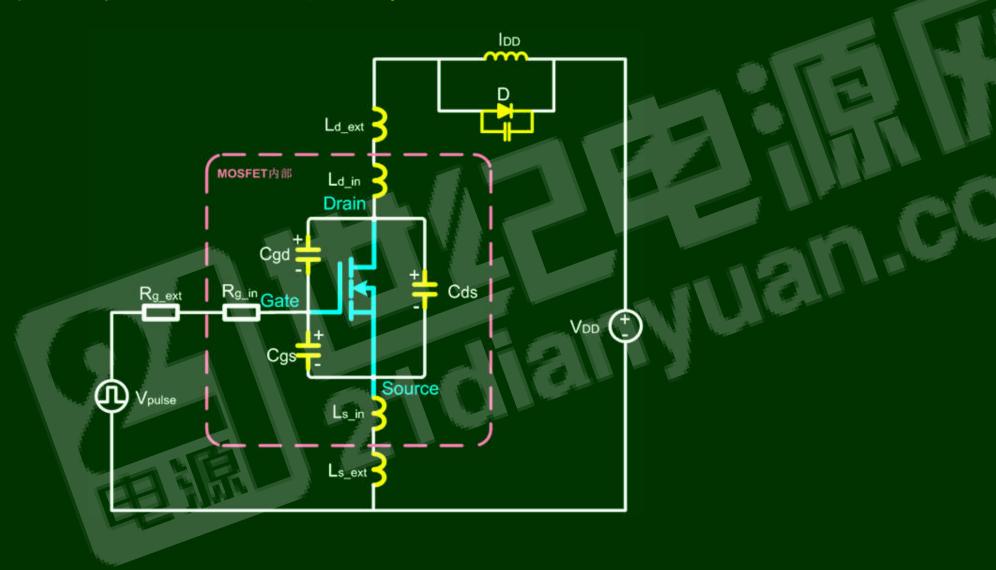


## MOSFET封装寄生电感



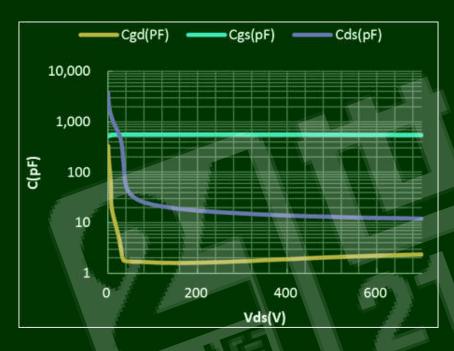


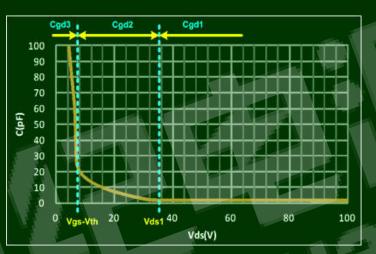
# 非理想状态下MOSFET开关过程

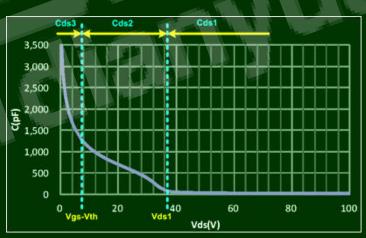




## MOSFET结电容和Vps强非线性

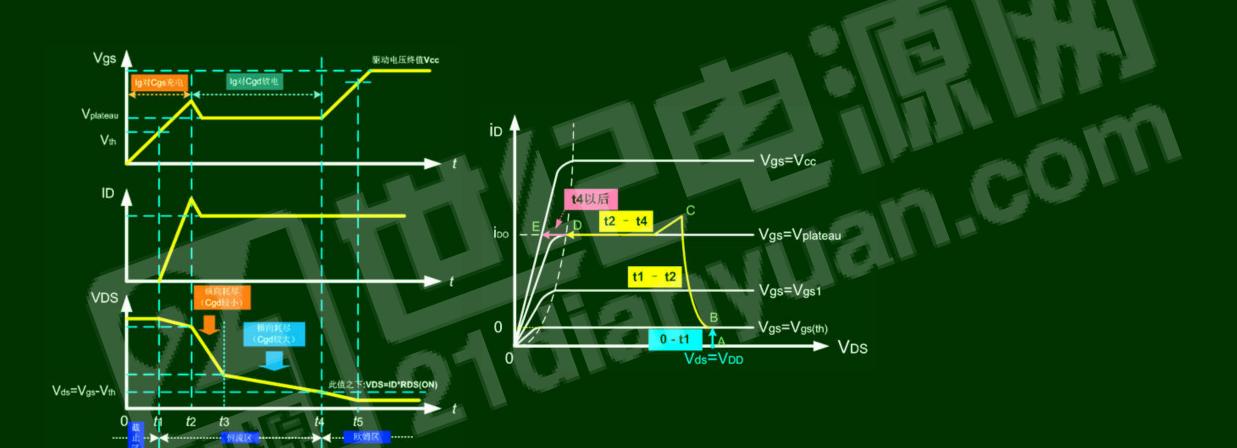






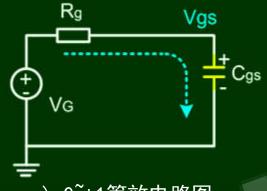


## 开通过程

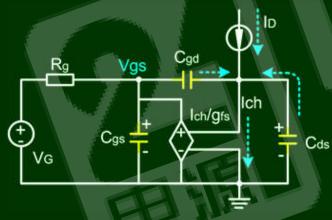




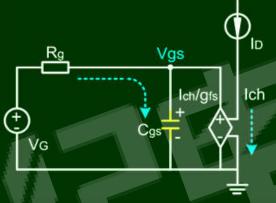
## 开通过程等效电路



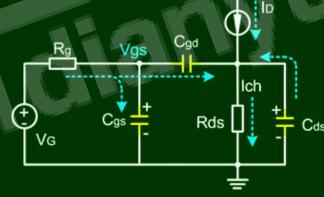




c)t2~t4等效电路图



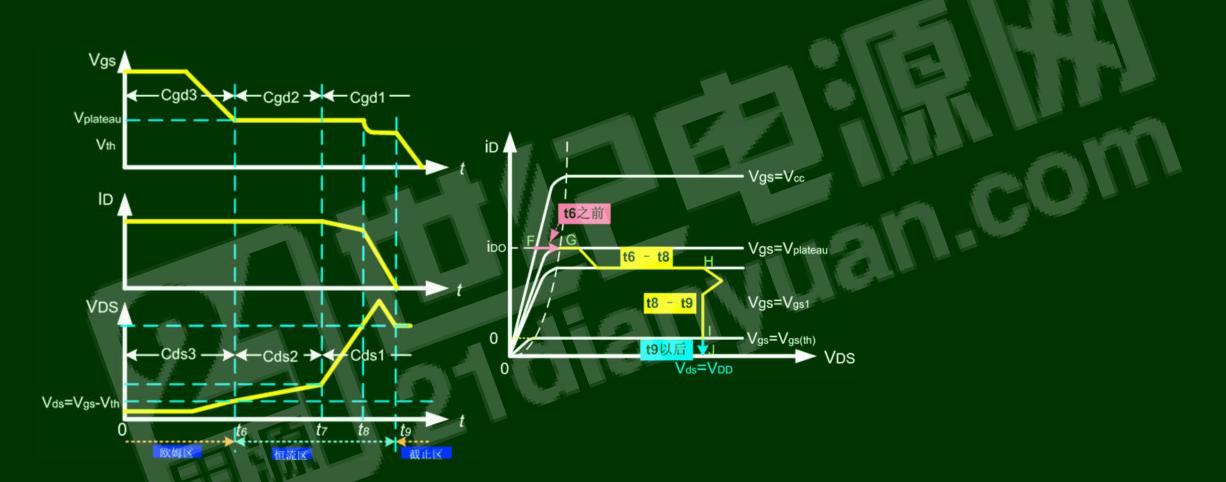
b)t1~t2等效电路图



d)t4以后等效电路图

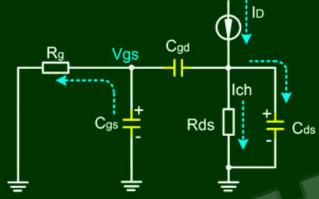


## 关断过程

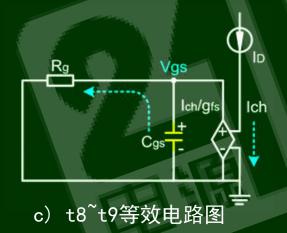


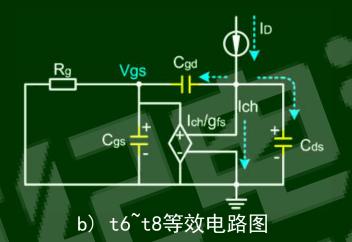


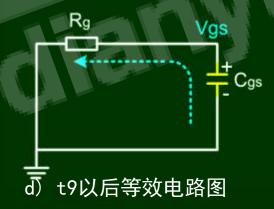
# 关断过程等效电路



a)t6之前等效电路图

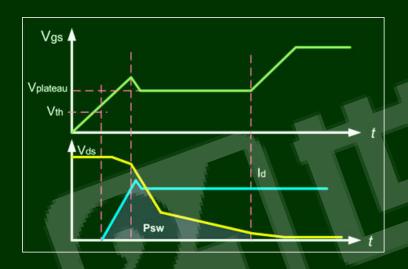




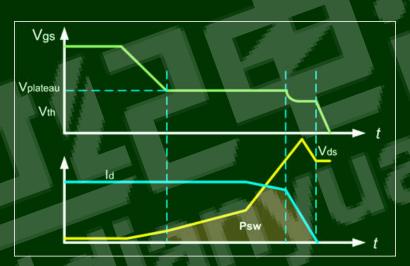




# 开关损耗的形成示意图



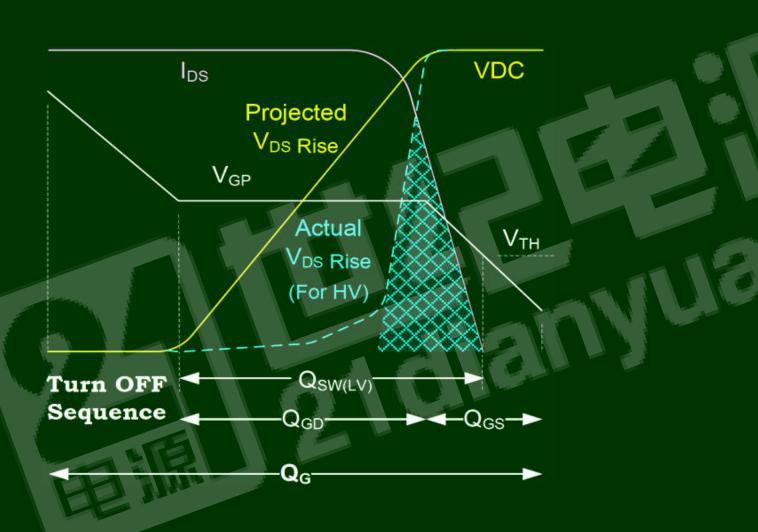
开通损耗示意图



关断损耗示意图

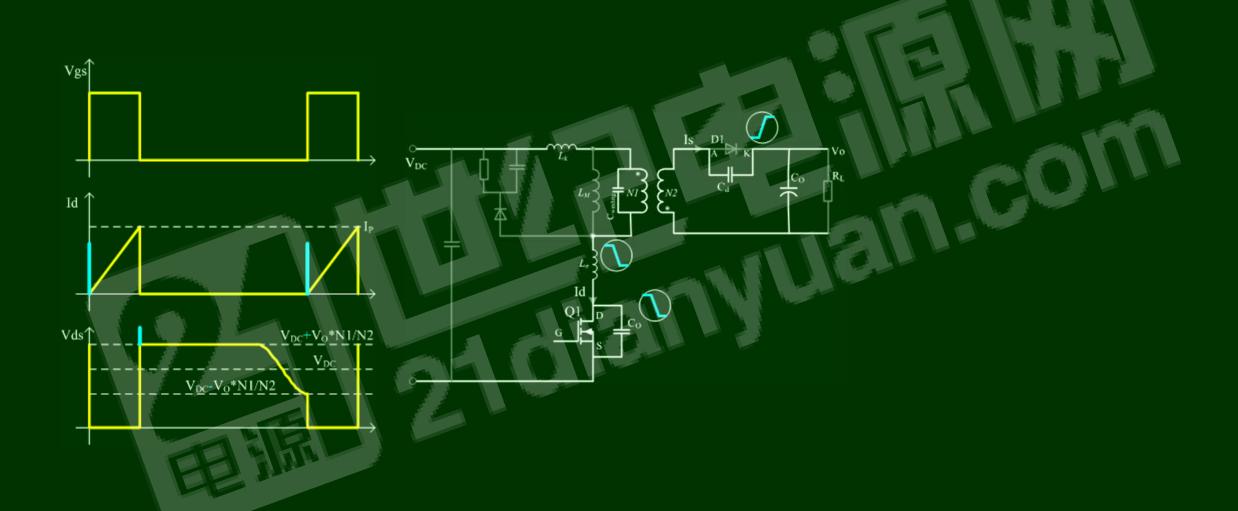


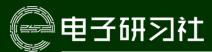
# 栅极电荷Qsw和损耗的关系(高压和低压两种情况)



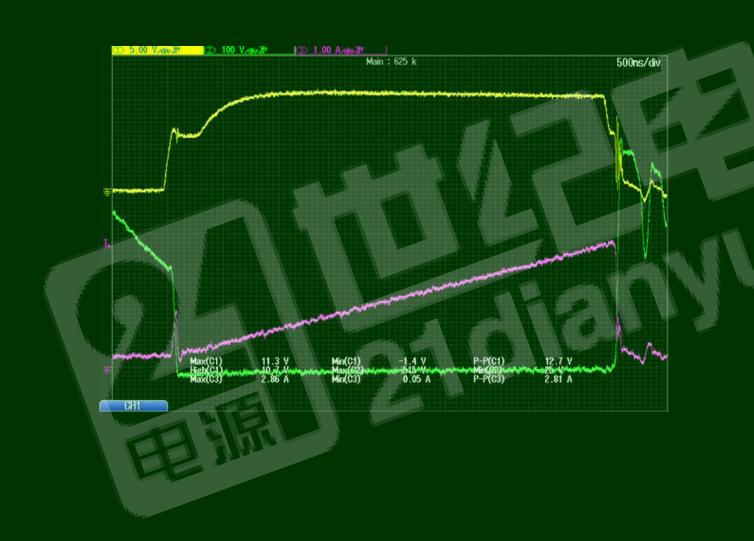


# 非理想状态下MOSFET开关过程(单端反激)



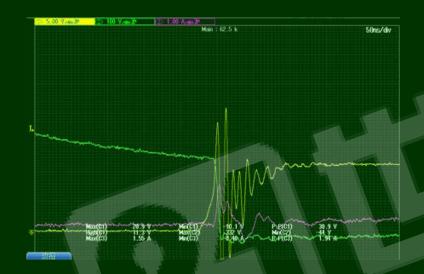


# 非理想状态下MOSFET开关波形(单端反激)

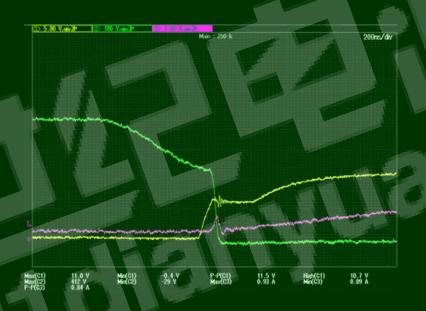




## 非理想状态下MOSFET开关波形(单端反激)



驱动开通电阻<mark>33Ω</mark> 驱动关断电阻16.5Ω



驱动开通电阻**100Ω** 驱动关断电阻16.5Ω



## 非理想状态下MOSFET开关波形(单端反激)



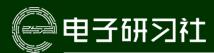


驱动开通电阻**33Ω** 驱动关断电阻16.5Ω 驱动开通电阻<mark>33Ω</mark> 驱动关断电阻16.5Ω

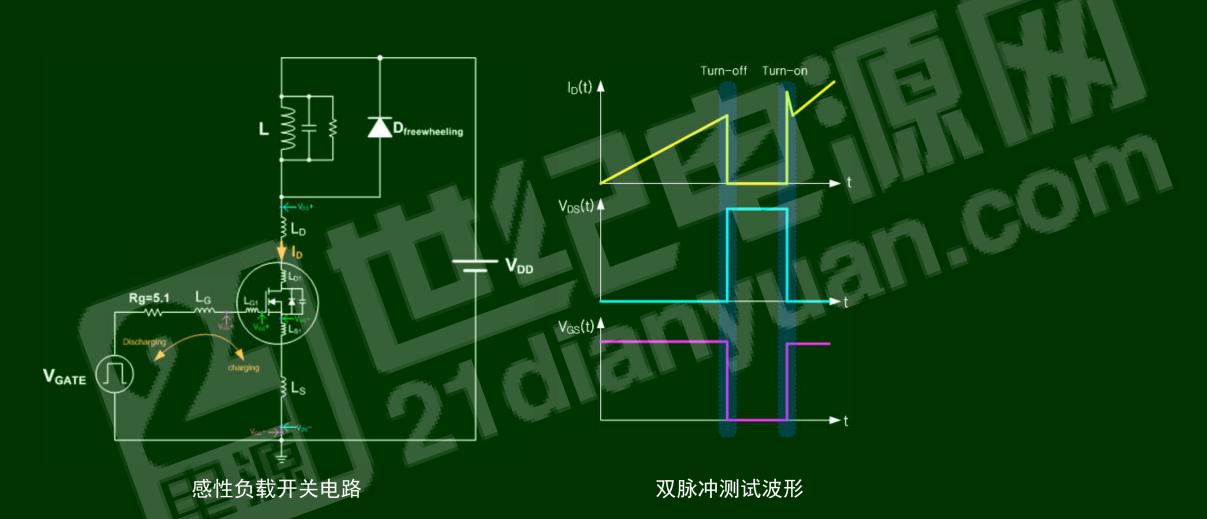


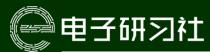
## 单端反激MOSFET开关波形



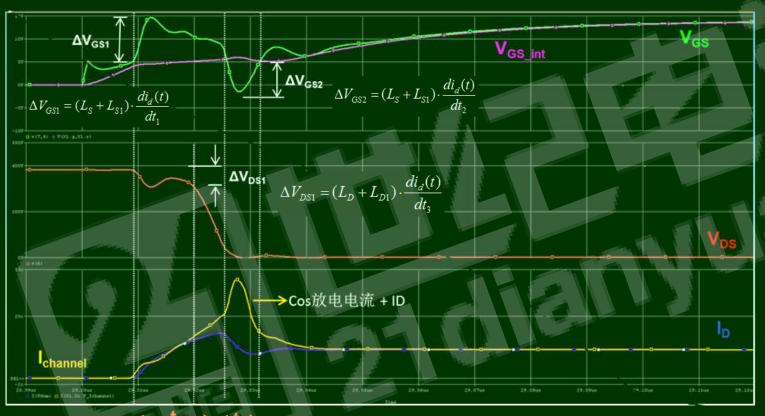


# 感性负载开关测试平台





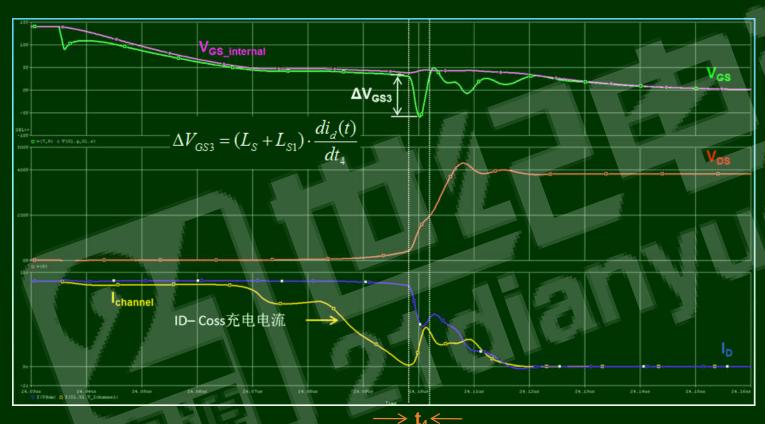
## MOSFET开通过程波形分析







## MOSFET关断过程波形分析

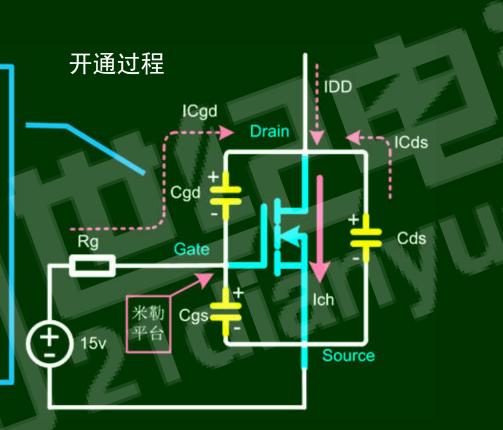






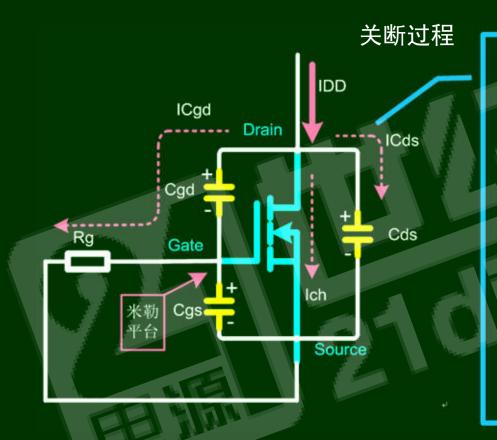
#### 栅源极电容Cds的影响— 示意图

开通时候的 dV/dt 基本由驱动电流 对 Cgd 的放电速度 决定。所以增加 Cds 对 Vds 的下降 速度影响不大,但 是会增加沟道电 流,增加开通损 耗。





#### 栅源极电容Cds的影响— 示意图

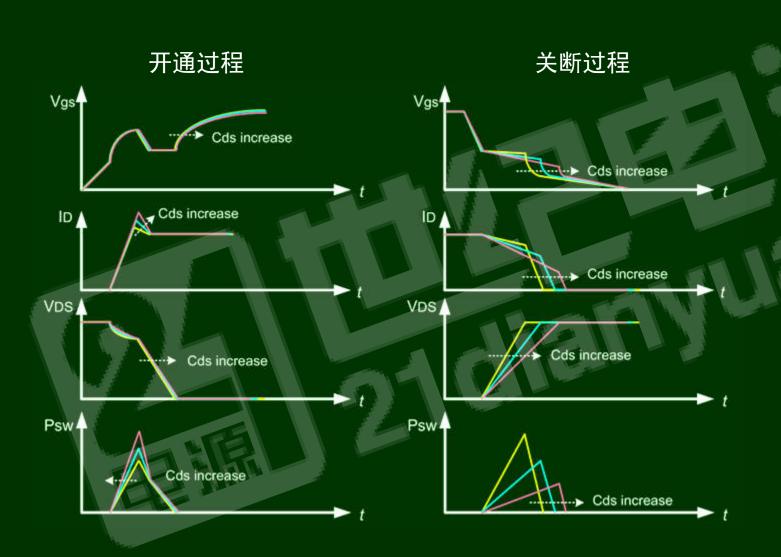


关断时候 IDD 一部分 用于给 Cds 充电, 一 部分用于给 Cgd 充 电, 剩余的部以 Vds 电, 剩途的,以 Vds 的上升速度由 Cds 和 Cgd 大小决使 Vds 上升变慢, 沟结电 上升变慢, 沟;时时 大人会变小,同时 大人会降低。



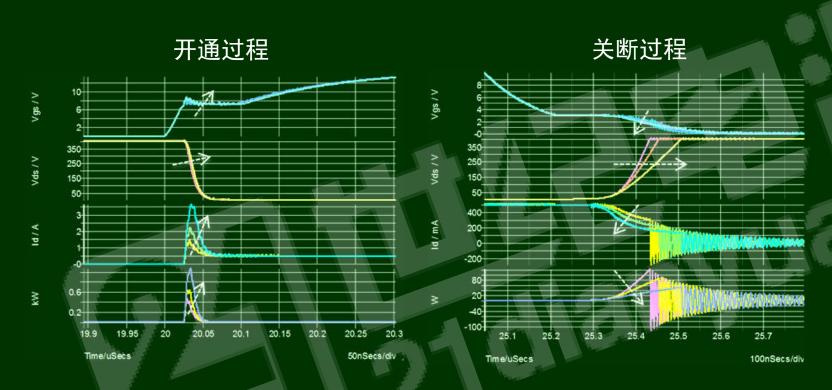


## 栅源极电容Cds的影响— 示意图





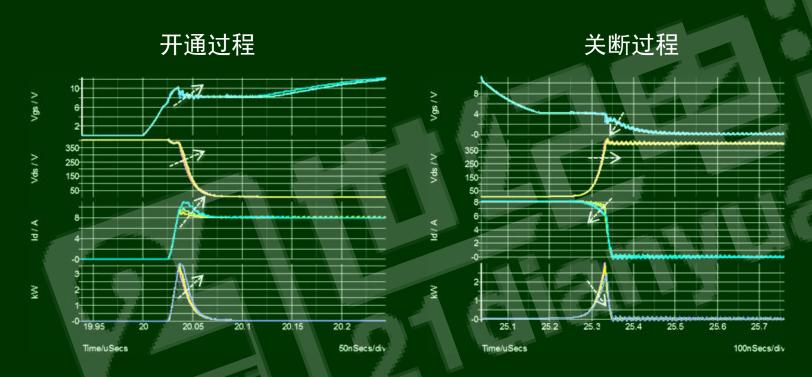
## 栅源极电容Cds的影响— 仿真图



Id=0.5A, 增加Cds对损耗和dv/dt影响比较明显



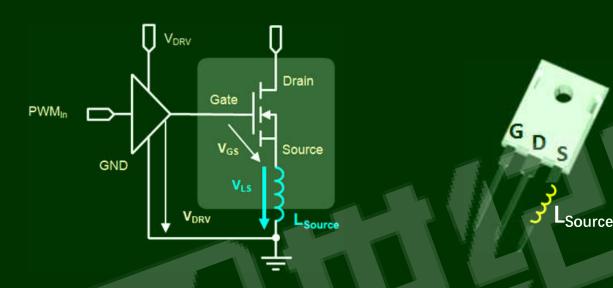
## 栅源极电容Cds的影响— 仿真图



Id=8A。增加Cds对损耗和dv/dt的影响不太明显。



#### 源极寄生电感Ls对开关损耗的影响



$$\begin{split} t_{on} &= \left(R_g \cdot C_{iss} + L_S \cdot g_{fs}\right) \cdot ln \left(\frac{V_{gon} - V_{gs(th)}}{V_{gon} - V_{gs(Miller)}}\right) + C_{rss} \cdot R_g \cdot \left(\frac{V_{ds} - V_{gs(Miller)}}{V_{gon} - V_{gs(Miller)}}\right) \\ P_{S.on} &= 0.5 \cdot I_{L.avg} \cdot V_o \cdot t_{on} \cdot f \end{split}$$

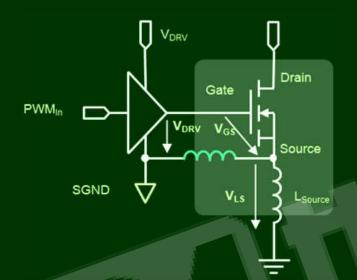
$$t_{off} = C_{rss} \cdot R_g \cdot \left(\frac{V_{ds} - V_{gs(Miller)}}{V_{gs(Miller)}}\right) + \left(R_g \cdot C_{iss} + L_S \cdot g_{fs}\right) \cdot ln\left(\frac{V_{gs(Miller)} - V_{g\_off}}{V_{gs(th)} - V_{g\_off}}\right)$$

$$P_{S.off} = 0.5 \cdot I_{L.avg} \cdot V_o \cdot t_{off} \cdot f$$

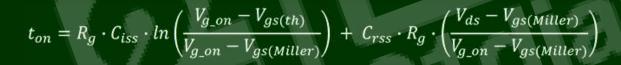
Ref: Application Note\_Practical design and evaluation of an 800 W PFC boost converter using TO-247 4pin MOSFET



## 源极寄生电感Ls对开关损耗的影响







$$t_{off} = C_{rss} \cdot R_g \cdot \left( \frac{V_{ds} - V_{gs(Miller)}}{V_{gs(Miller)}} \right) + R_g \cdot C_{iss} \cdot ln \left( \frac{V_{gs(Miller)} - V_{goff}}{V_{gs(th)} - V_{goff}} \right)$$

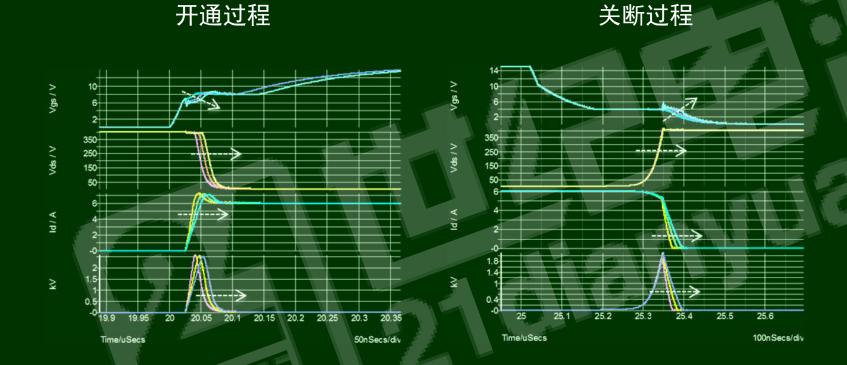


TO-Leadless





## 源极寄生电感Ls对开关损耗的影响





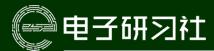
# 主要内容

• 功率MOSFET的原理

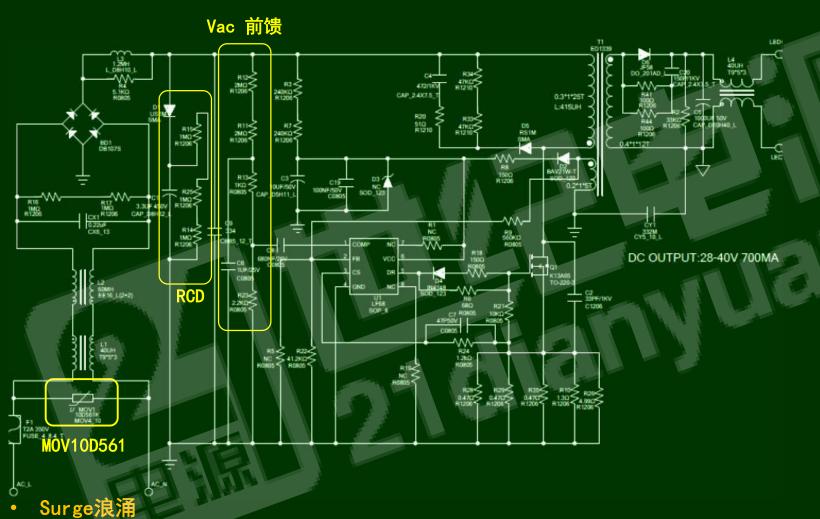
• 功率MOSFET的参数和特性

• 功率MOSFET的开关过程分析

• 功率MOSFET的典型应用分析



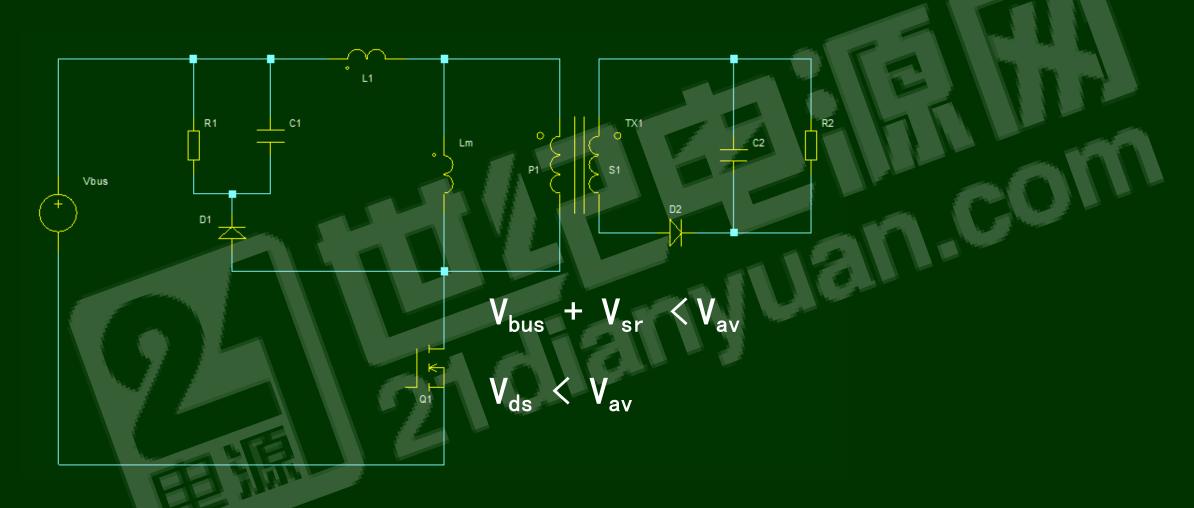
## LED电源



- 输入电压突变

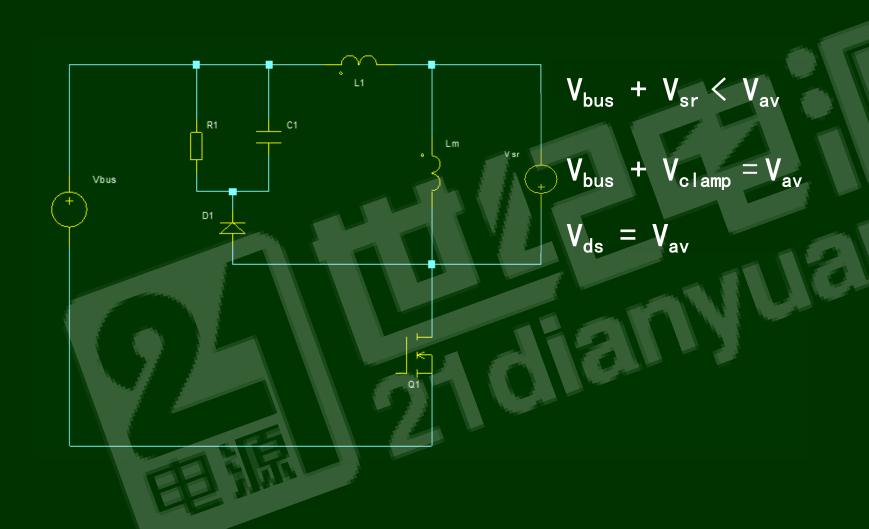


## 简化后的Flyback Case 1



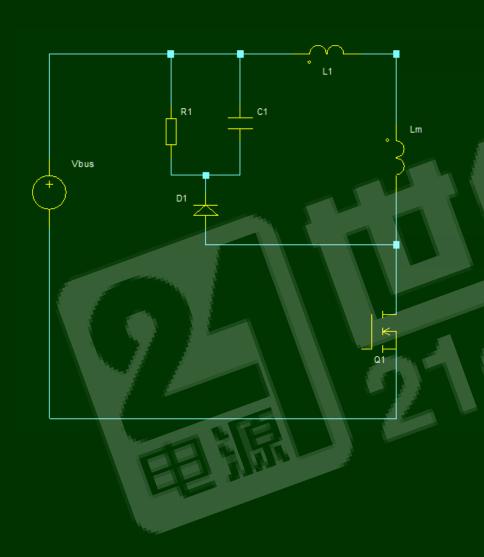


# 简化后的Flyback Case 2



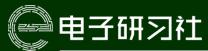


## 简化后的Flyback Case 3



$$V_{bus} + V_{sr} > V_{av}$$

$$V_{ds} = V_{av}$$



### MOSFET雪崩过程中失效



图: 浪涌测试波形

输入电压:230Vac/50Hz,输出: 32W

通道1: MOS 漏源电压(黄色, 200V/每格);

通道2: Z2 母线电压(绿色, 200V/每格);

通道3:MOS 漏源电流(粉色, 5A/每格);

Time: 10µs/每格



#### 差模浪涌Surge改善对策



 $U_{av} > U_{busmax}$ 

差模浪涌Surge 改善方法

提升MOSFET的雪崩 能力

改善变压器饱和度

 $U_{inpk} \cdot T_{on} = N \cdot B \cdot Ae$   $L_p \cdot I_p = N \cdot B \cdot Ae$ 

增加变压器匝数 N 减小MOSFET开通时间 Ton

增加变压器磁通面积 Ae

变压器Core变大,和原来的Bobbin不匹配

减小原边绕组的截面积, 增加导通损耗 减小原边激磁电感Lp,通 过略微增加气隙, 开关频率增加,开关损耗 增加



### MOSFET雪崩能力

Characteristics		Symbol	Rating	Unit
Drain-source voltage		VDSS	650	V
Gate-source voltage		V <sub>GSS</sub>	±30	V
Drain current	DC (Note 1)	ID	13	A
	Pulse (Note 1)	I <sub>DP</sub>	26	
Drain power dissipation (Tc = 25°C)		PD	40	W
Single pulse avalanche energy (Note 2)		Eas	86	mJ
Avalanche current		IAR	13	А
Repetitive avalanche energy (Note 3)		E <sub>AR</sub>	4.0	mJ

Note 2:  $V_{DD}$  = 90 V,  $T_{ch}$  = 25 °C (initial), L = 0.9 mH,  $R_G$  = 25  $\Omega$ ,  $I_{AR}$  = 13 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature





#### Surge Case 3

# 700mA/32W LED PS Single stage Flyback

# 必要条件: U<sub>av</sub> > U<sub>busmax</sub>



LSD11N70浪涌测试波形

输入电压:230Vac/50Hz,输出: 32W

通道1: MOS 漏源电压(黄色, 200V/每格);

通道2: Z2 母线电压(绿色, 200V/每格);

通道3:MOS漏源电流(粉色, 5A/每格);

Time: 5µs/每格

漏源电压=820√ 浪涌电压1400√90⁰测试波形

母线电压=883V



**700mA/32W LED PS**Single stage Flyback



LSD11N70浪涌测试波形

输入电压:230Vac/50Hz,输出: 32W

通道1: MOS 漏源电压(黄色, 200V/每格);

通道2: Z2 母线电压(绿色, 200V/每格);

通道3:MOS漏源电流(粉色, 5A/每格);

Time: 5µs/每格

漏源电压=848V 浪涌电压1400V/90º测试波形

母线电压=801V 最大漏源电流=5.8A



700mA/32W LED PS Single stage Flyback



\*\*\*11N70浪涌测试波形

输入电压:230Vac/50Hz,输出: 32W

通道1: MOS 漏源电压(黄色, 200V/每格);

通道2: Z2 母线电压(绿色, 200V/每格);

通道3:MOS漏源电流(粉色, 5A/每格);

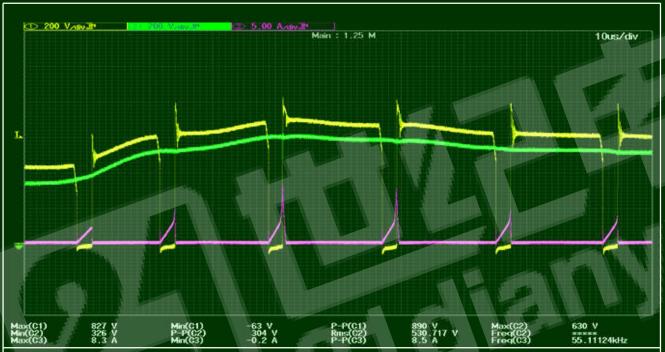
Time: 5µs/每格

漏源电压=832V 浪涌电压1400V/90º测试波形

母线电压=805V 最大漏源电流=8.3A



■ Vac=230V, 浪涌电压=600V



### LSD07N65-1运行波形

通道1: MOS 漏源电压(黄色, 200V/div); 通道2: 电源母线电压(绿色, 200V/div);

通道3:: MOS 漏源电流(黄色, 5A/div);

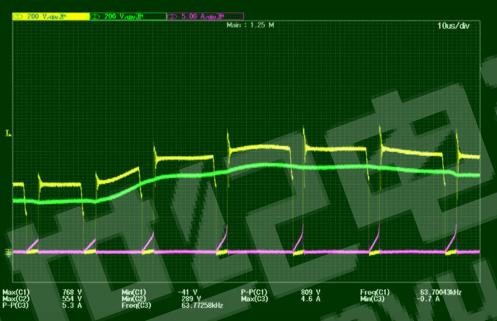
时间: 10µs/div Idmax=8.3A





700mA/32W LED PS Single stage Flyback

压敏电阻22



LSD07N65 浪涌测试波形

输入电压:230Vac/50Hz, 输出: 32W

通道1: MOS 漏源电压(黄色, 200V/每格);

通道2: Z2 母线电压(绿色, 200V/每格);

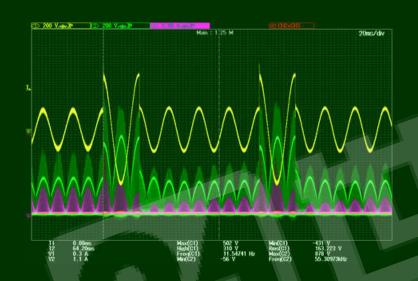
通道3:MOS漏源电流(粉色,5A/每格);

Time: 10µs/每格

漏源电压=763V 浪涌电压2000V/90º测试波形

母线电压=535V 最大漏源电流=4.6A

### 输入电压突变 Case 2



Input voltage:100V-300Vac/50Hz

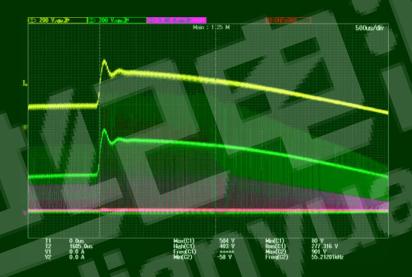
CH1: Vin (yellow, 200V/div);

CH2: MOS VDS (green, 5V/div);

CH3:MOS IDS (purple, 5A/div);

Time: 20ms/div

### **Single stage Flyback LED PS**



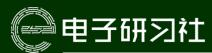
Input voltage:100V-300Vac/50Hz

CH1: Vin (yellow, 200V/div);

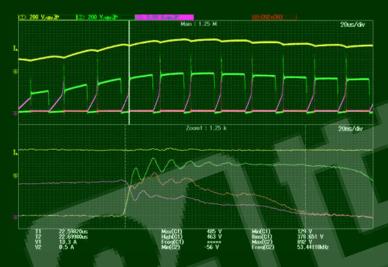
CH2: MOS VDS (green, 5V/div);

CH3:MOS IDS (purple, 5A/div);

Time: 500us/div



### 输入电压突变 Case 2



#### LSD11N70

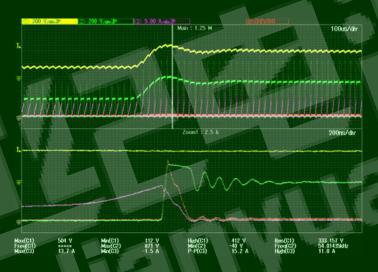
CH1: Vin (yellow, 200V/div);

CH2: MOS VDS (green, 5V/div);

CH3:MOS IDS (purple, 5A/div);

Time: 20us/div 20ns/div ZOOM

### **Single stage Flyback LED PS**



#### \*\*\*15NM65N

CH1: Vin (yellow, 200V/div);

CH2: MOS VDS (green, 5V/div);

CH3:MOS IDS (purple, 5A/div);

Time: 100us/div 200ns/div ZOOM



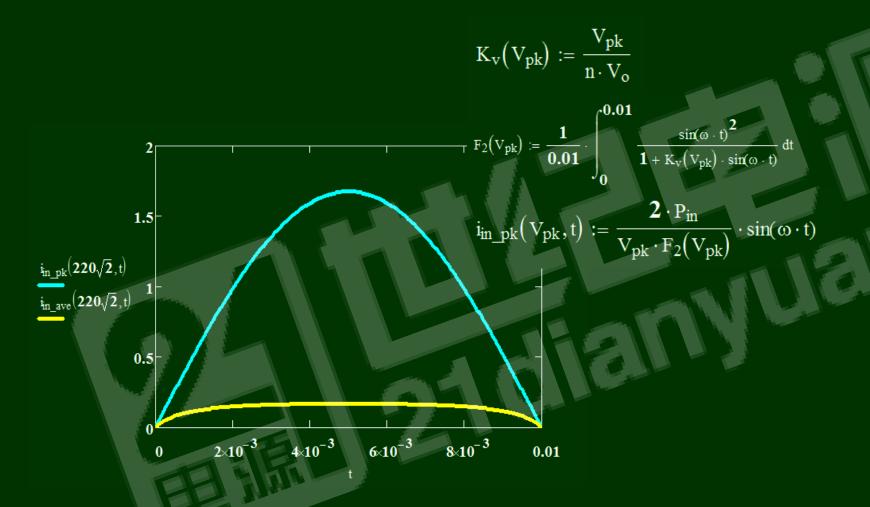
### 整改前surge电流波形(220Vac, 1300V/90°)





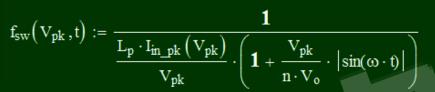


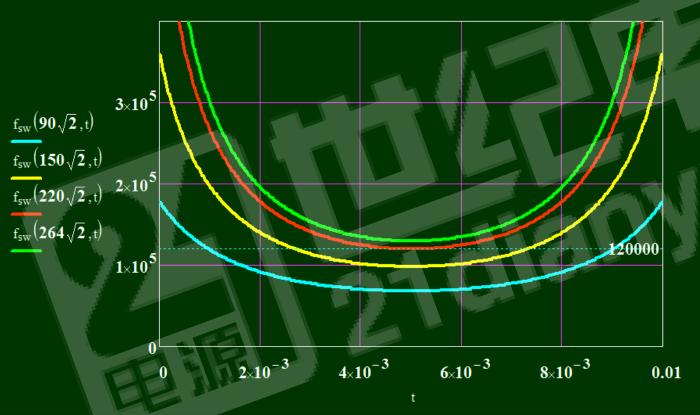
## CRM Flyback 基本关系

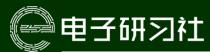




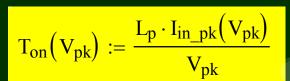
## CRM Flyback 基本关系

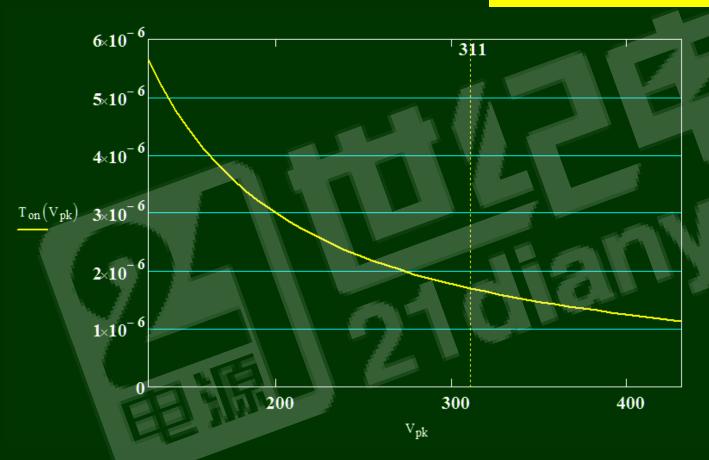






## CRM Flyback 基本关系



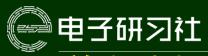




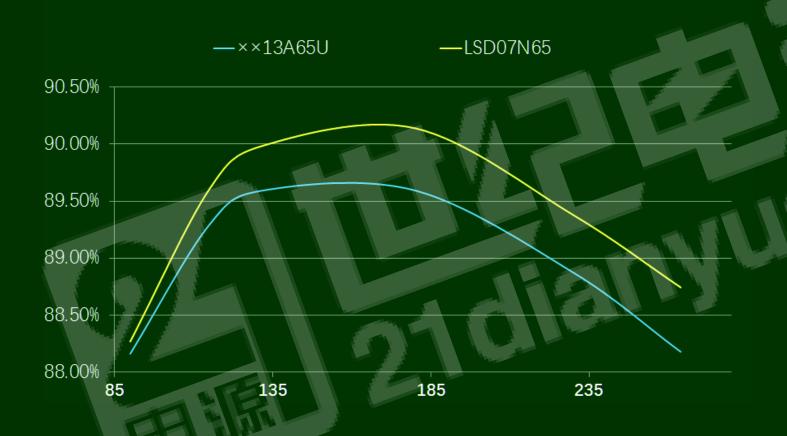
整改后surge电流波形(220Vac, 1300V/90°)



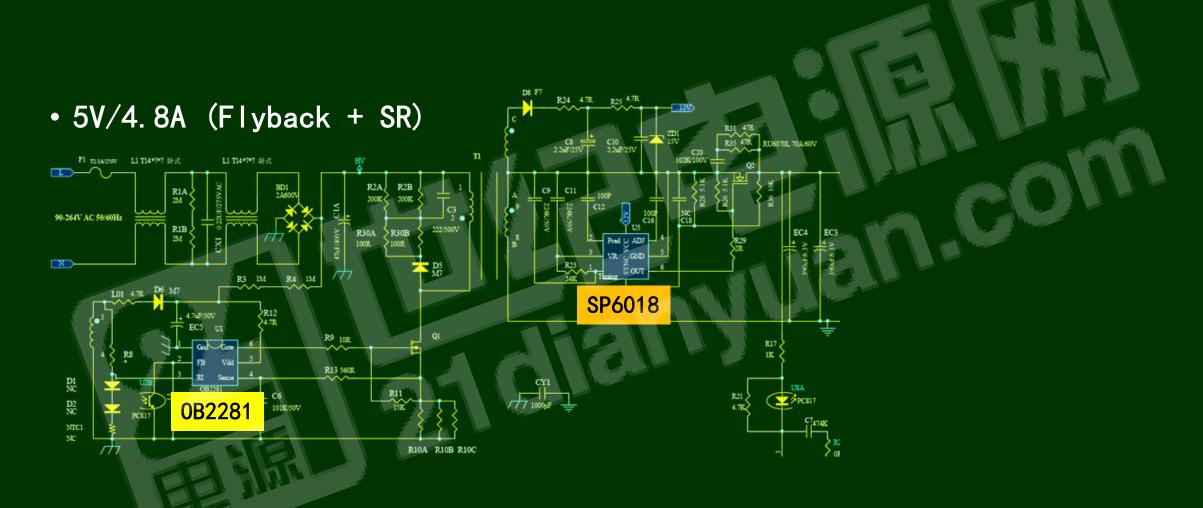




## 效率对比









#### Oscillator Operation

During the full load power operation, OB2281 operates at a 65KHz (typical) fixed frequency. The efficiency and system cost is controlled at an optimal level. A peak power mode is implemented to supply a peak current output requirement. In peak power mode, frequency is increased from 65KHz (typical) to 142KHz (typical).

At light load levels, OB2281 enters the light load mode, where the output current is reduced. The switching losses are reduced by lowering the switching frequency.



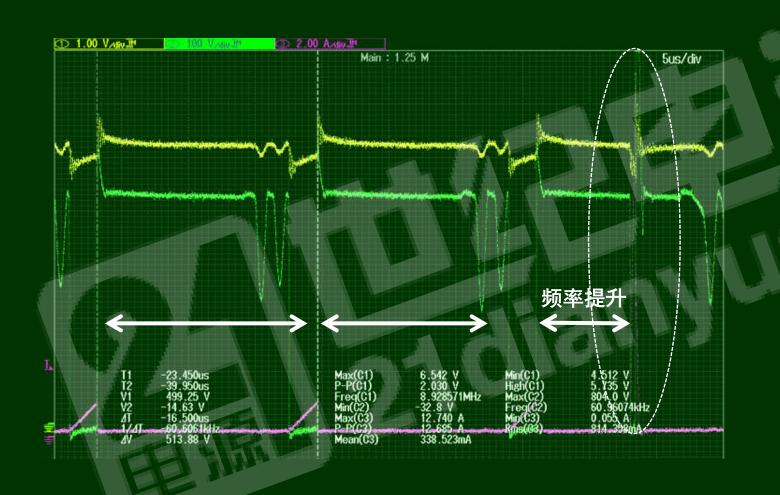


#### DESCRIPTION

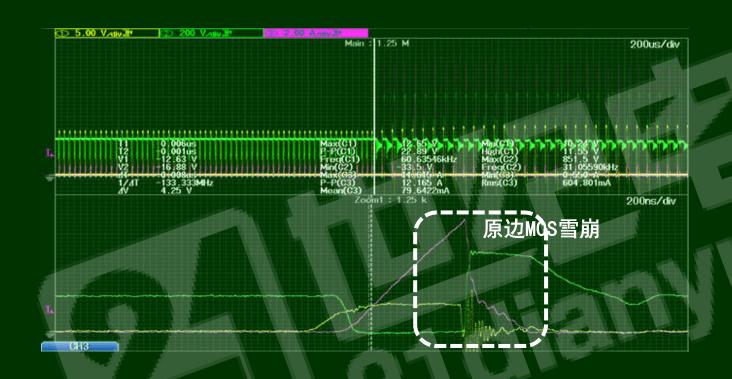
The fundamental of SP6018 synchronous rectifier (SR) driver IC is based on our U.S. patented methods that utilize the principle of "prediction" logic circuit. The IC deliberates previous cycle timing to control the SR in present cycle by "predictive" algorithm that makes adjustments to the turn-off time, in order to achieve maximum efficiency and avoid cross-conduction at the same time. Specially, SP6018 is designed for Resonance. It also maintains the MOSFET's body diode conduction at minimum level. The SP6018 is capable to adapt in almost all existing Resonance converters with few adjustments considered necessary.







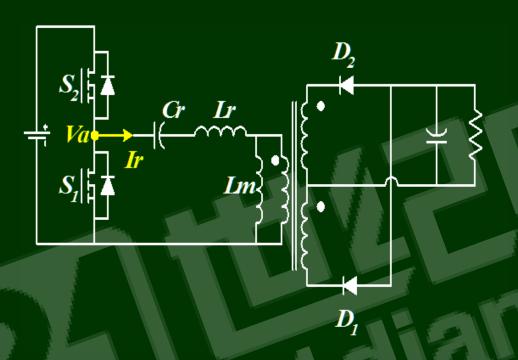




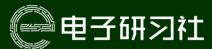
负载切换: 空载-满载(5V-4.8A) MOSFET IDSmax=11.615A. Vdsmax=851V CH1 Vgs, CH2 Vds, CH3 lds.



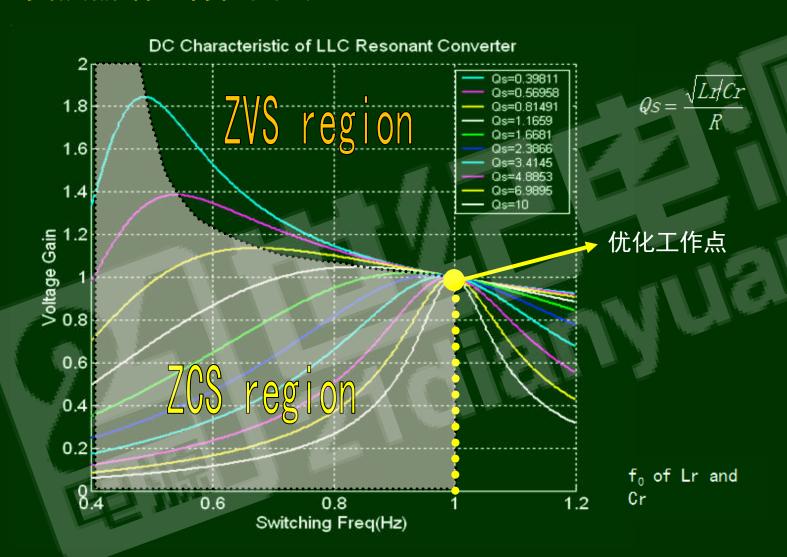
## LLC 谐振变换器



- · ZVS, 高效率, 高频化
- 副边整流二极管电压应力低,无反向恢复问题
- 全负载范围内实现原边MOSFET ZVS

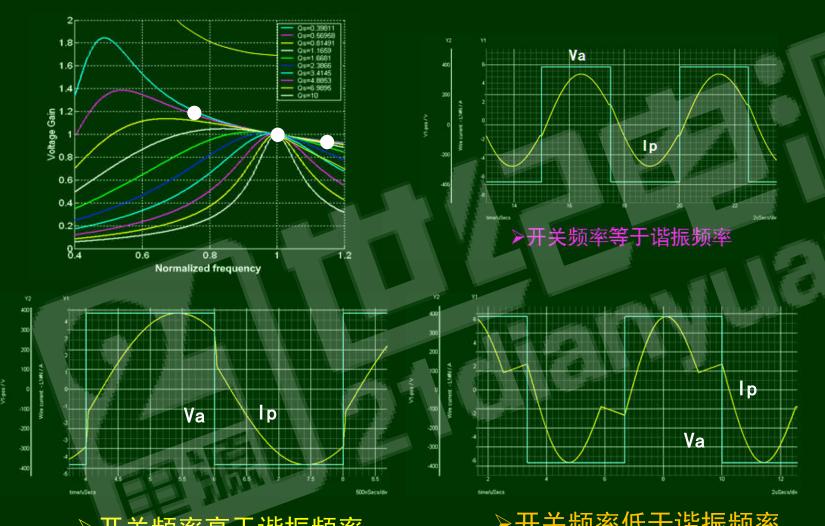


## LLC变换器增益特性曲线





# 不同开关频率情况下LLC工作波形

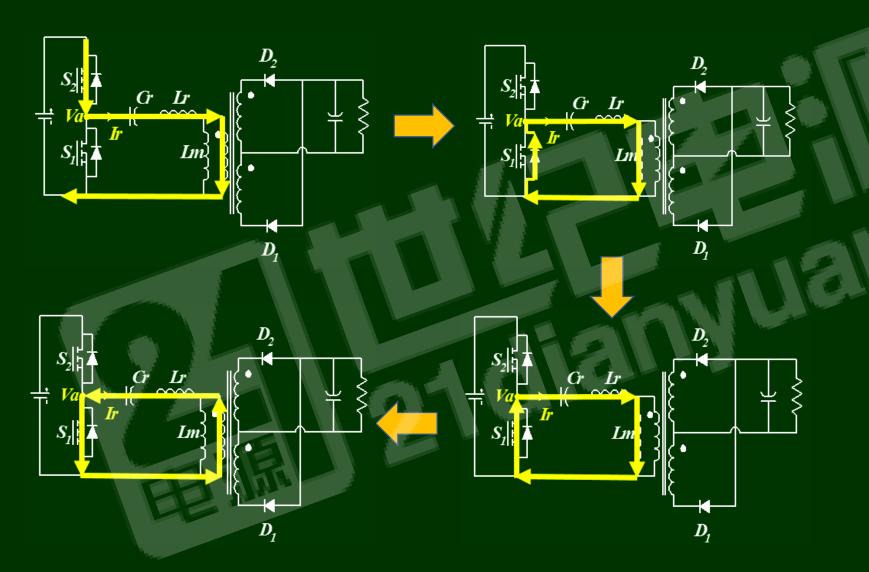


▶开关频率高于谐振频率

▶开关频率低于谐振频率

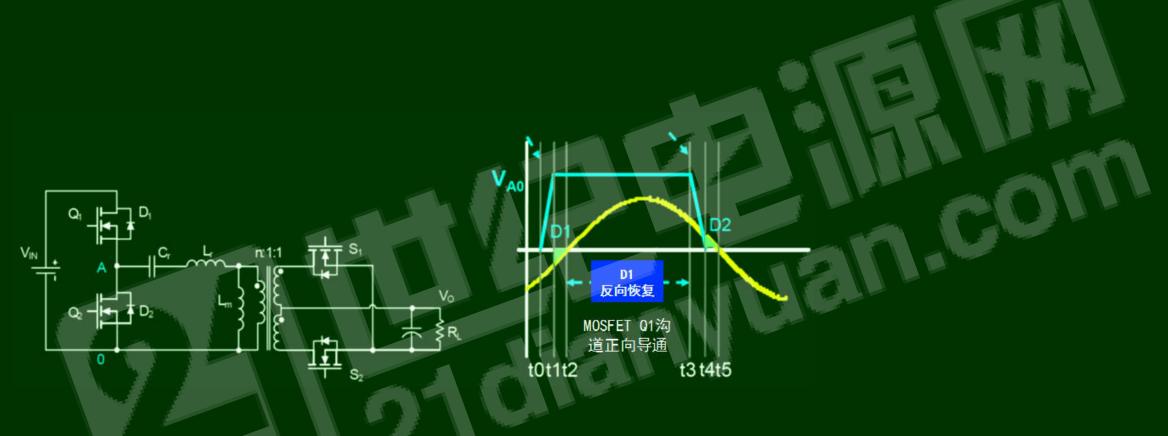


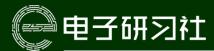
## LLC变换器 ZVS状态下模态切换



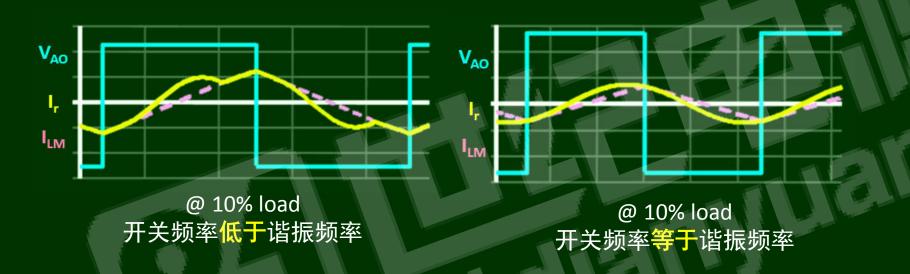


# LLC变换器工作波形(ZVS模式)





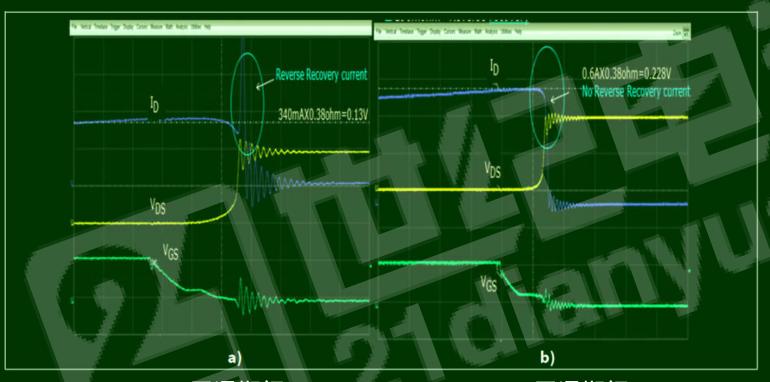
## LLC变换器工作波形(ZVS模式, 轻载)



Clark Person, Selection of Primary Side Devices for LLC Resonant Converters, CPES Thesis



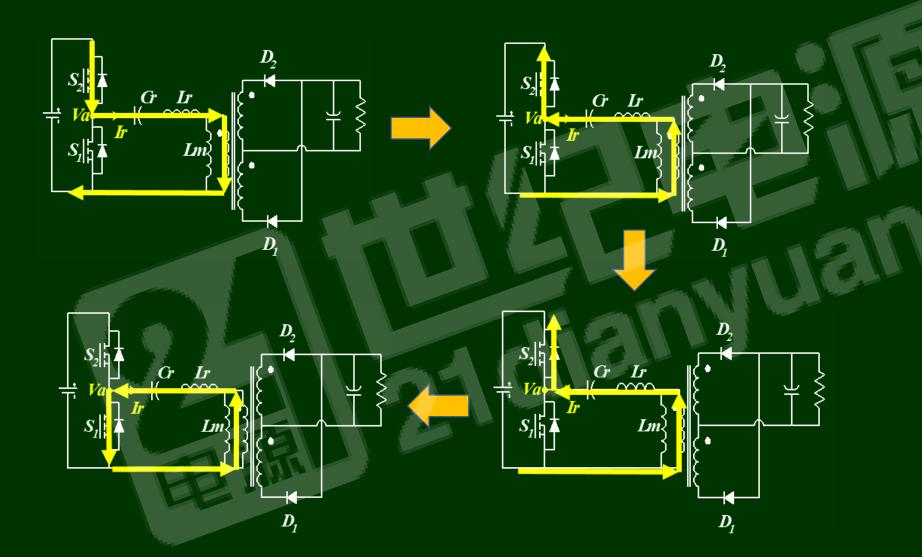
# LLC变换器工作波形(ZVS模式, 轻载)



MOSFET开通期间 体二极管没有完全恢复 MOSFET开通期间 体二极管完全恢复

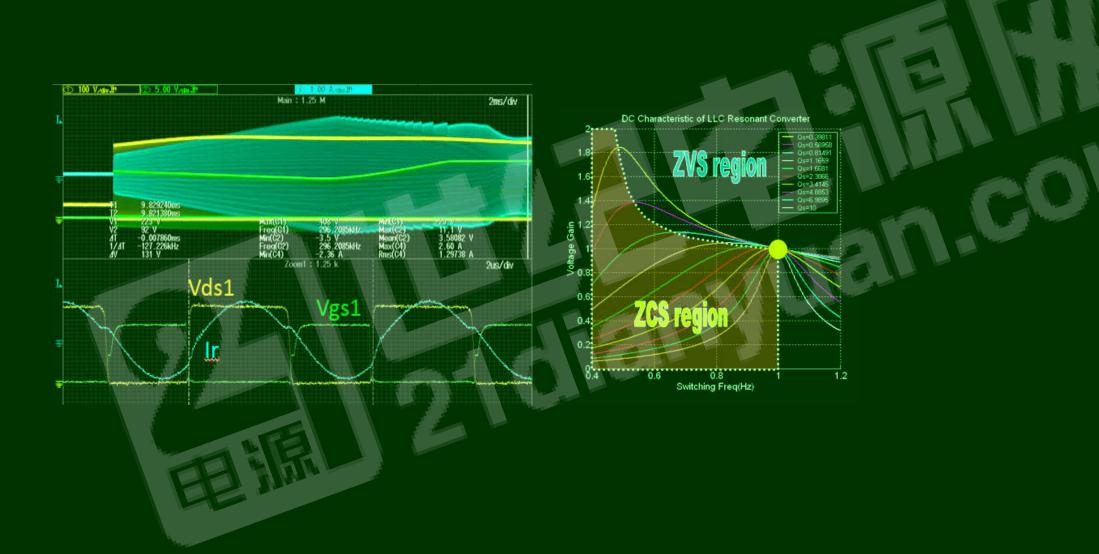


## LLC变换器 ZCS状态下模态切换





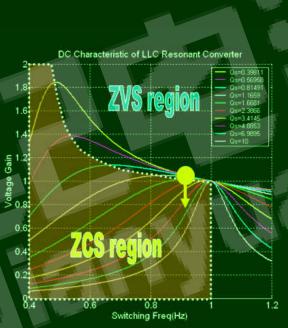
# LLC变换器工作波形

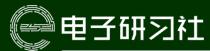




# LLC变换器工作波形

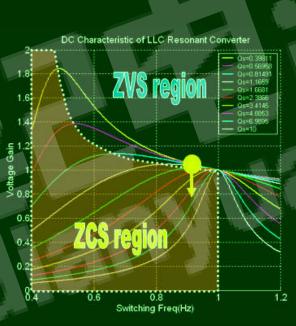






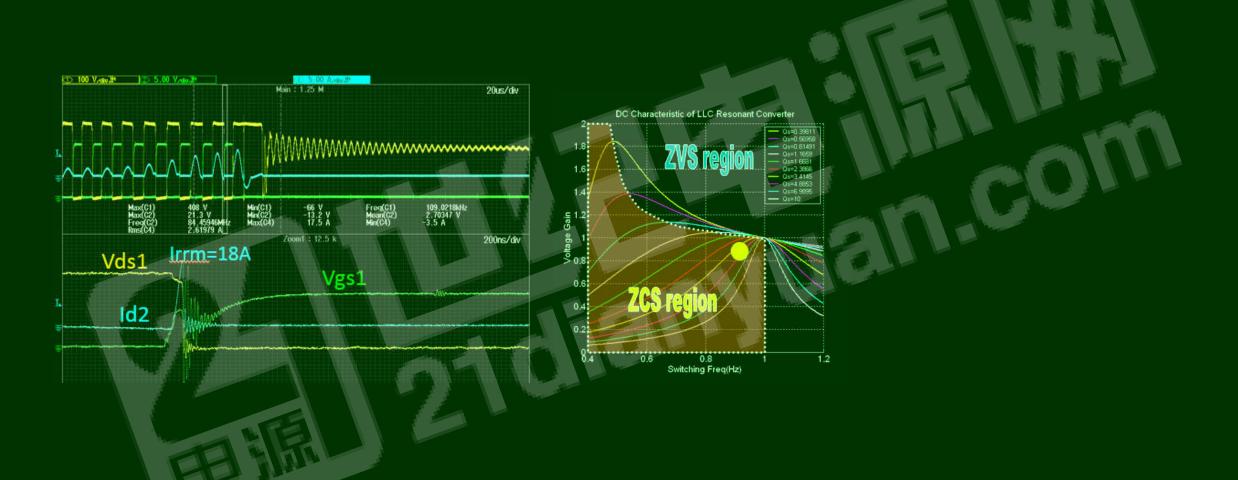
## LLC变换器输出短路状态1波形

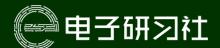




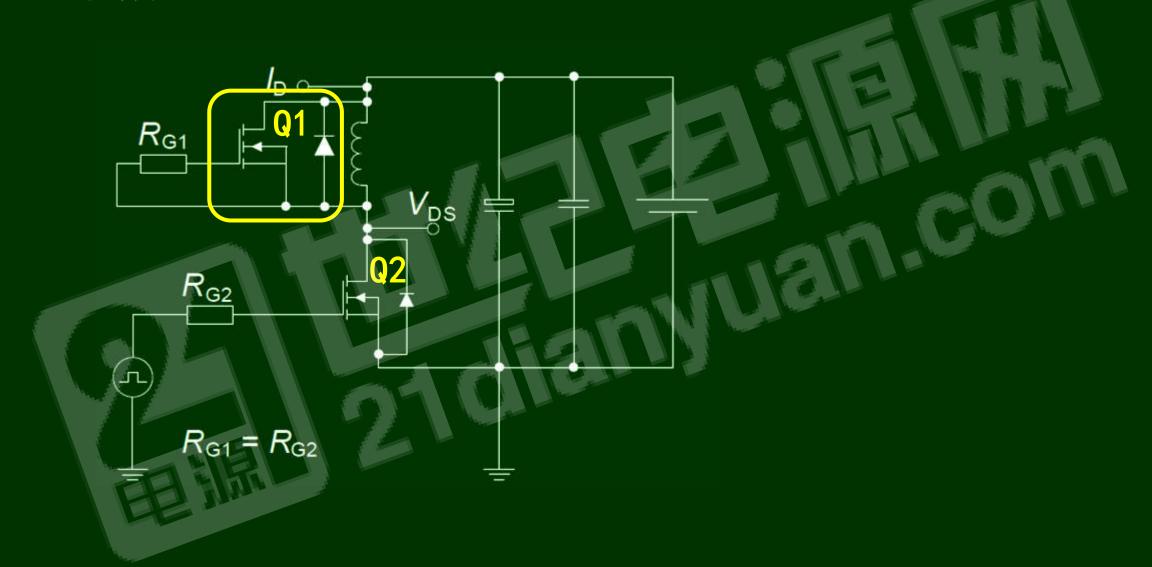


## LLC变换器输出短路状态2波形



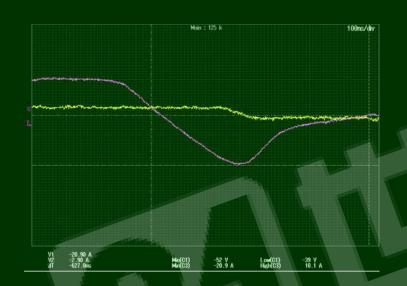


# 二极管特性测试电路





## SJ VDMOS Vs. 普通VDMOS体二极管特性对比

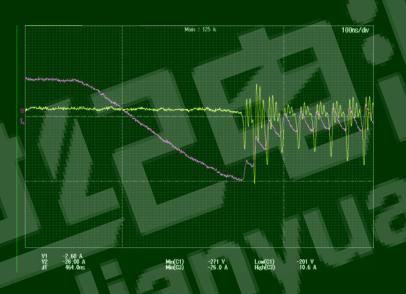


#### 普通 VDMOS 20A

CH1: VDS 100V/div; CH3: ISD 10A/div

Time: 100ns/div

 $I_F=10A$ ,  $di_F/dt=100A/us$ ,  $V_{DD}=50V$ 



#### SJ VDMOS 20A

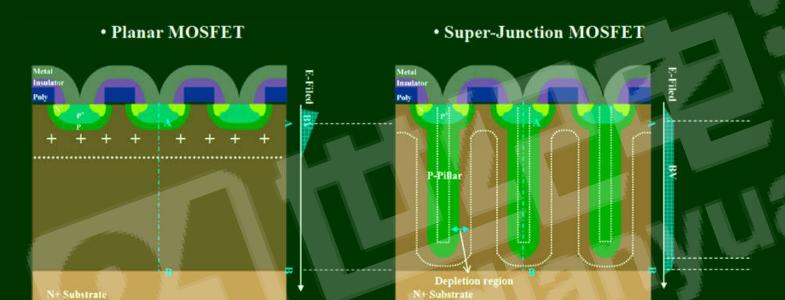
CH1: VDS 100V/div; CH3: ISD 10A/div

Time: 100ns/div

IF=10A,  $di_F/dt=100A/us$ , VDD=50V



## VD MOS 和SJ MOS的耗尽过程



 $Ron, sp = 6 \times 10^{-9} BV^{2.5}$ 

$$Ron, sp = \frac{cp.BV}{2q\mu E.Q}$$



## SJ MOSFET体二极管反向恢复特性(1)

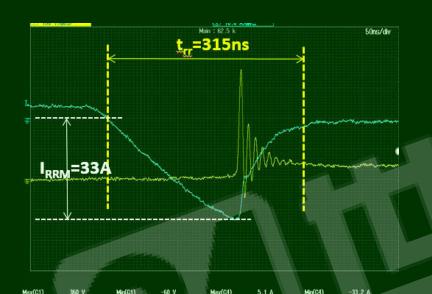
CH1: VDS 100V/div; CH3: ISD 10A/div Time: 100ns/div

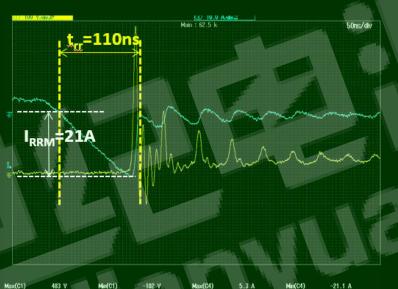






## 二极管反向恢复测试波形





#### **LSC20N65**

CH1: VDs 100V/div; CH4: ISD

5A/div

Time: 50ns/div

IF=5.1A, Rg=51 $\Omega$ , VDD=50V

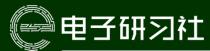
### LSC20N65F

CH1: VDs 100V/div; CH4: ISD

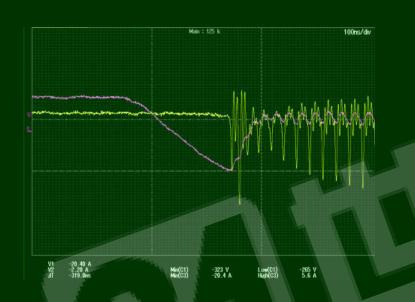
5A/div

Time: 50ns/div

IF=5.1A, Rg=51 $\Omega$ , VDD=50V



## Lonten 标准系列 Vs. E 系列 SJ MOS体二极管特性

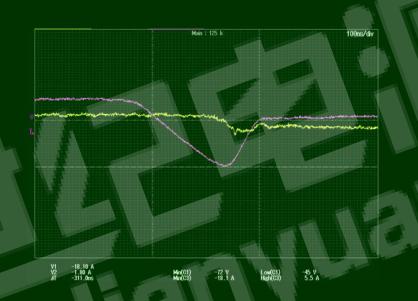


### **LSD11N65**

CH1: VDs 100V/div; CH3: IsD 10A/div

Time: 100ns/div

IF=5.5A, di<sub>F</sub>/dt=100A/us, VDD=50V



#### LSD11N65E

CH1: VDs 100V/div; CH3: ISD 10A/div

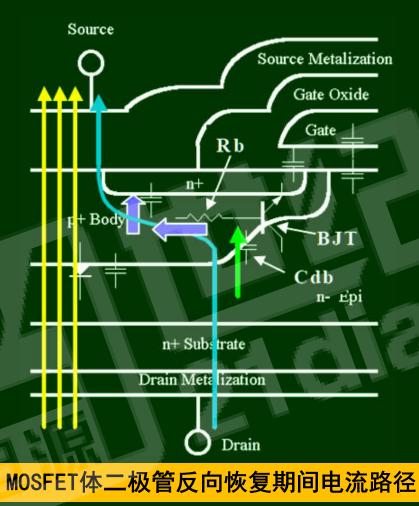
Time: 100ns/div

IF=5.5A,  $di_F/dt=100A/us$ , VDD=50V

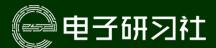


## MOSFET体二极管反向恢复电流路径

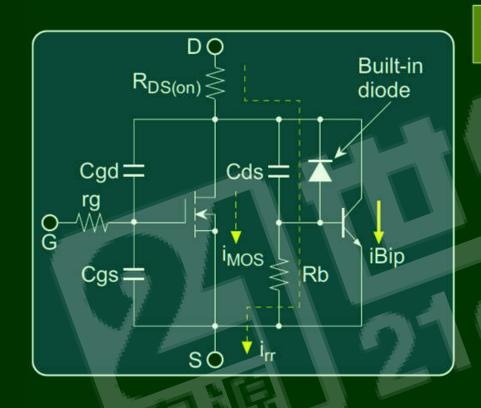
(位移电流、反向恢复电流、雪崩电流)



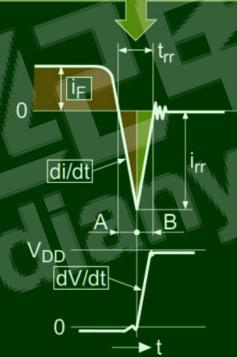




## 体二极管dv/dt能力及反向恢复导致的失效机理

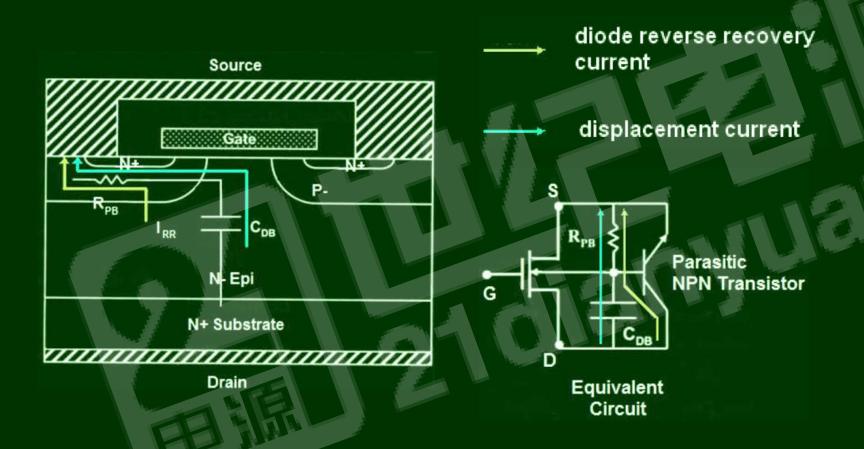


Destruction occurs while the diode voltage is recovering.





#### 体二极管dv/dt能力及反向恢复导致的失效机理





#### 二极管反向恢复过程定量关系

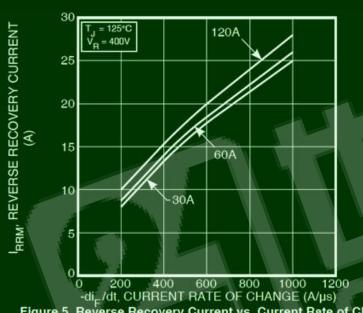
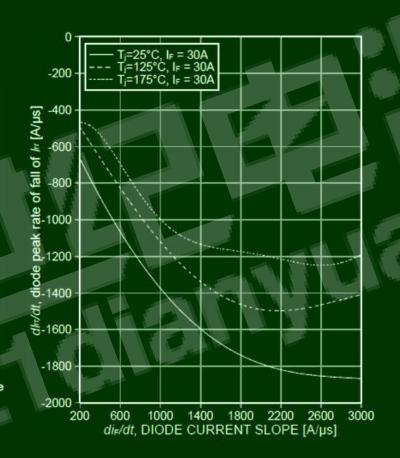


Figure 5. Reverse Recovery Current vs. Current Rate of Change





# LLC启动(CM6901)

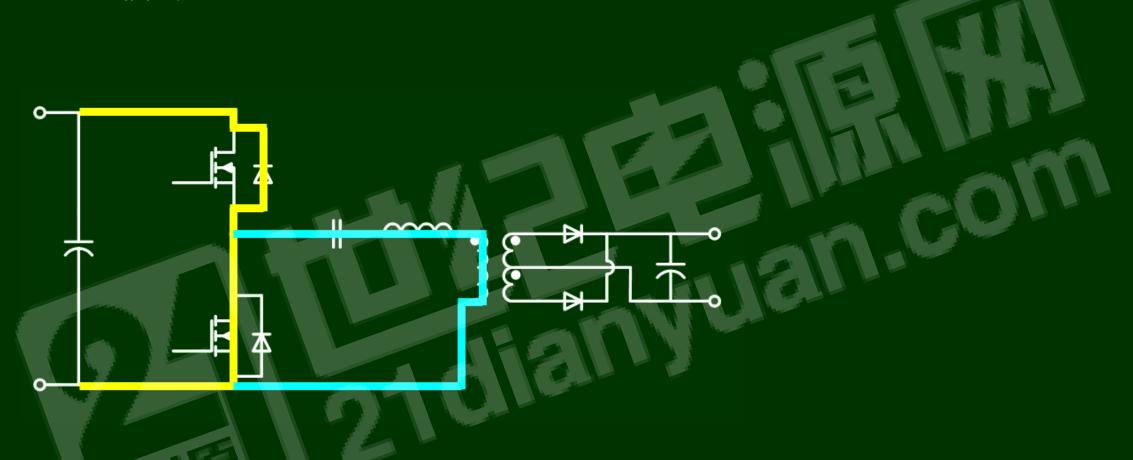
- 600W PC 电源 Gold
  - 前级采用Boost PFC
  - 后级采用LLC DC-DC (CM6901)



- CM6901
  - SRC/LLC + SR resonant controller
  - FM + 2 PWMING Mode Operation

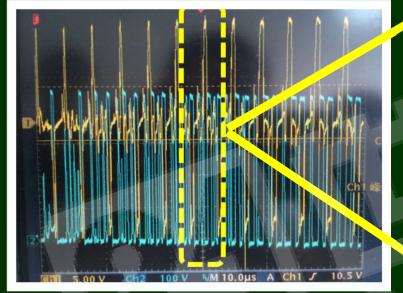


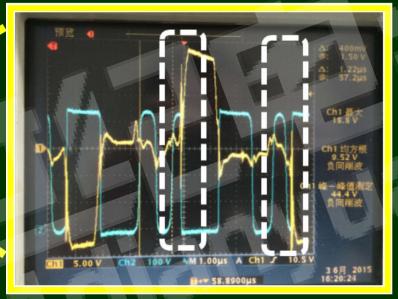
# LLC PWM模式(CM6901)





# LLC PWM模式启动波形





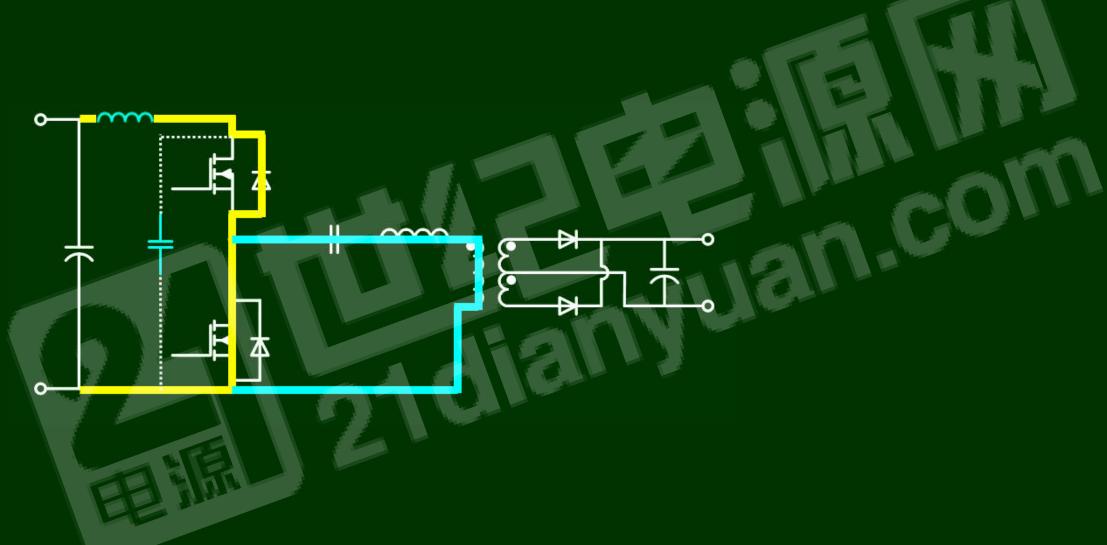
启动过程图

启动过程细节图

通道1: 下管 Vgs波形 通道2: 下管 Vds波形

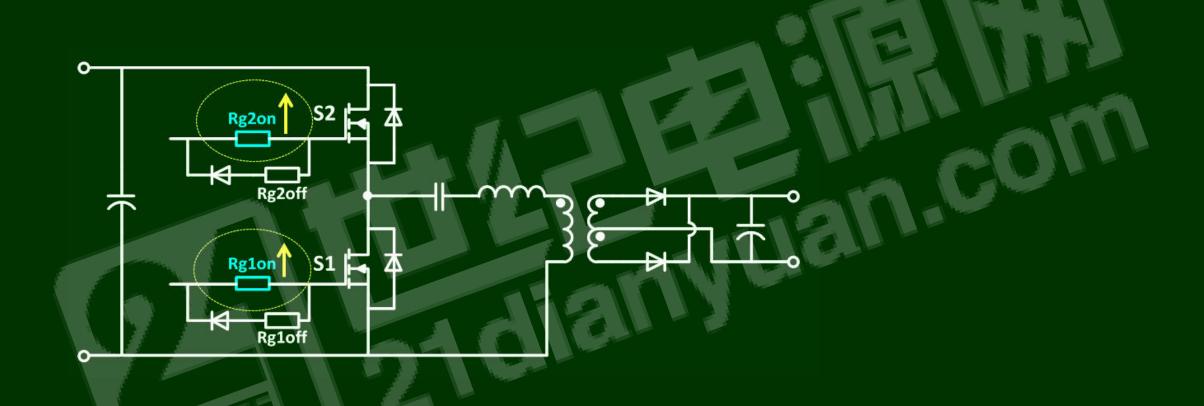


# LLC PWM模式(CM6901)



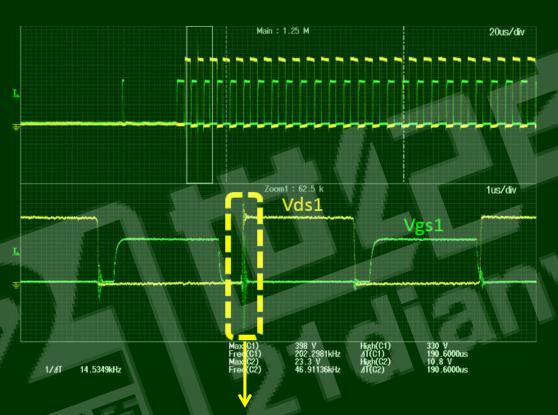


# 如何减缓二极管反向恢复

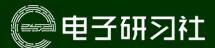




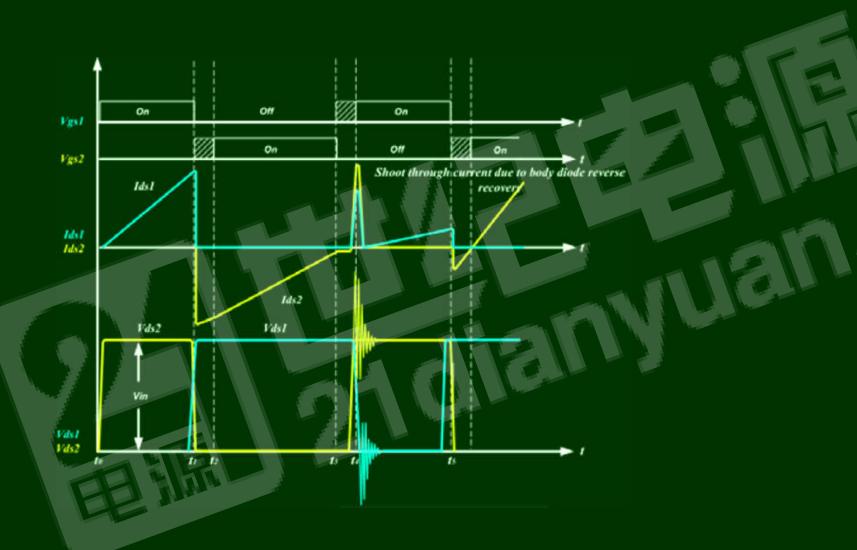
#### LLC 启动波形 (L6599)

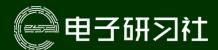


上管开通时刻,下管MOS体二极管反向恢复,导致驱动波形和Vds波形出现强烈振荡。

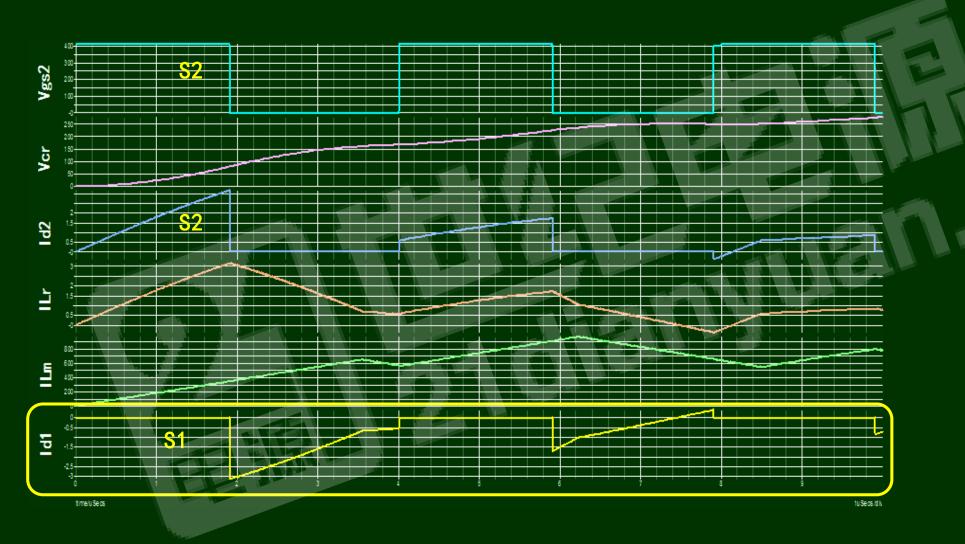


# LLC启动过程 - MOS体二极管反向恢复(示意图)



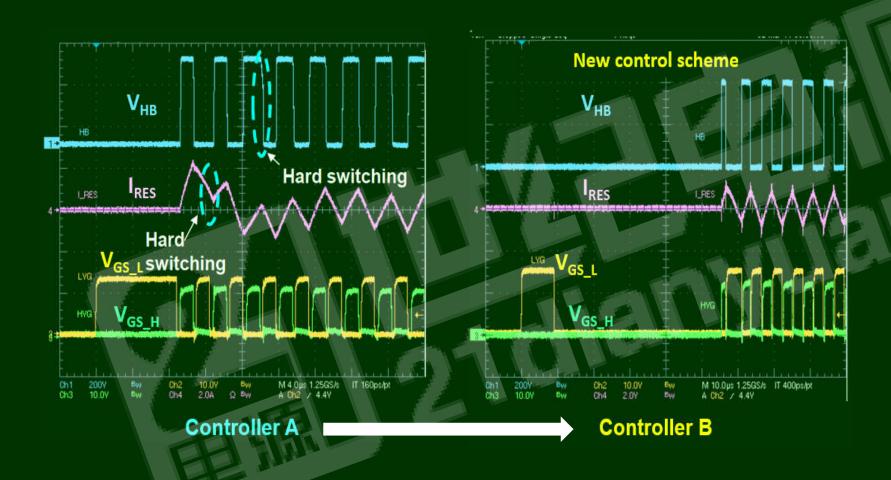


# LLC启动过程 - MOS体二极管反向恢复(仿真波形)



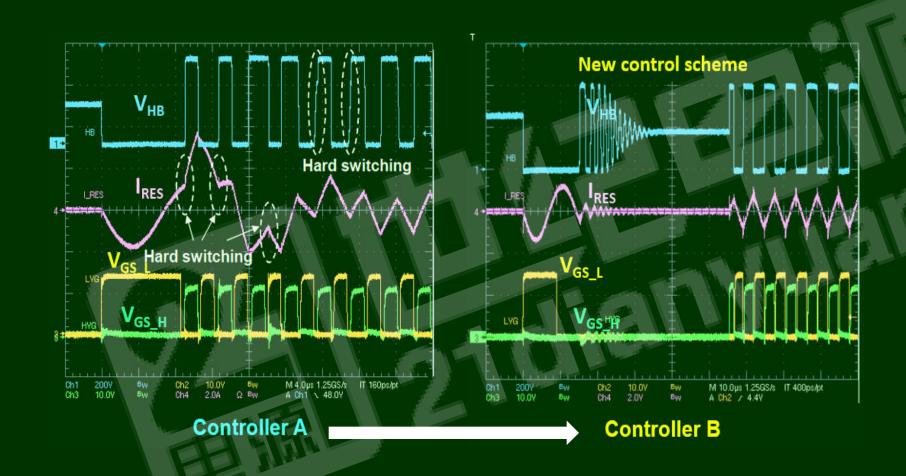


# 如何消除二极管反向恢复(启动过程)





# 如何消除二极管反向恢复(快速ON-OFF-ON-OFF-···)





# 低压MOSFET的体二极管特性

#### **Drain-Source Diode Characteristics**

#### 40V/80A/2. 1mΩ 低压MOSFET

V <sub>SD</sub>	Source to Drain Diode Voltage	I <sub>SD</sub> = 35A	Į į	0.8	1.25	V
	Source to Drain Diode voltage	I <sub>SD</sub> = 15A		0.8	1.0	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 35A, di/dt = 100A/μs	1 - T	52	68	ns
Q <sub>rr</sub>	Reverse Recovery Charge	I <sub>F</sub> = 35A, di/dt = 100A/μs	- 1	76	99	nC

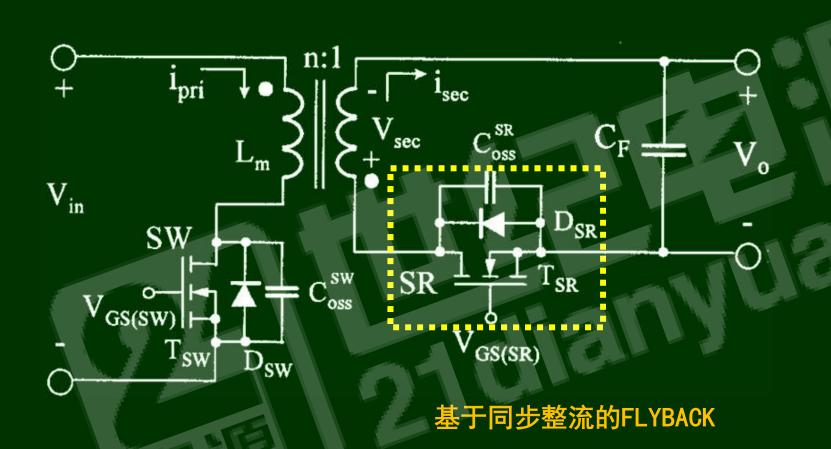
#### **Reverse Diode**

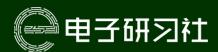
#### 80V/120A/2. 8mΩ 低压MOSFET

Diode continous forward current	Is	-T <sub>C</sub> =25 °C	•		100	Α
Diode pulse current	/ <sub>S.pulse</sub>	7 c-23 0			400	
Diode forward voltage	V <sub>SD</sub>	V <sub>GS</sub> =0 V, I <sub>F</sub> =100 A, T <sub>j</sub> =25 °C		1.0	1.2	٧
Reverse recovery time	t <sub>m</sub> V <sub>R</sub> =40 V, I <sub>F</sub> =I <sub>S</sub> ,		20	113	2	ns
Reverse recovery charge	Q <sub>rr</sub>	d <i>i</i> <sub>F</sub> /d <i>t</i> =100 A/µs	-	317	-	nC

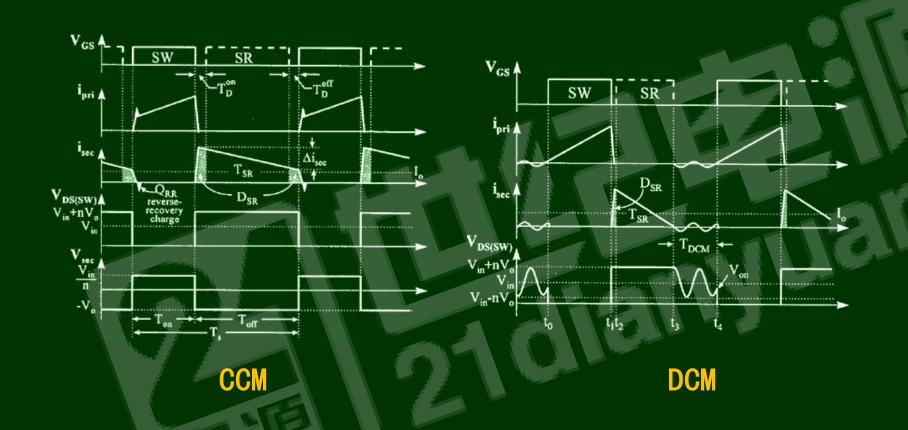


# 基于同步整流的FLYBACK



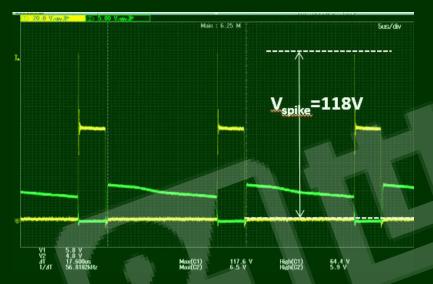


# 基于同步整流的FLYBACK的典型波形



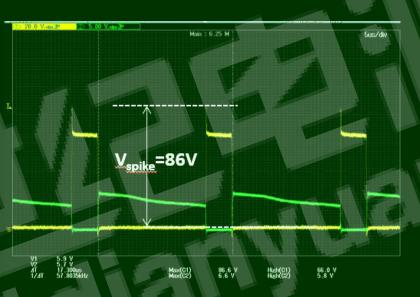


#### FLYBACK的同步整流MOS波形



通道1: SR MOS漏源电压Vds (黄色, 20V/DIV) 通道2: SR MOS门极驱动Vgs (绿色, 5V/DIV)

> 原边高压MOSFET驱动电阻 Rgon=47<mark>欧姆</mark>

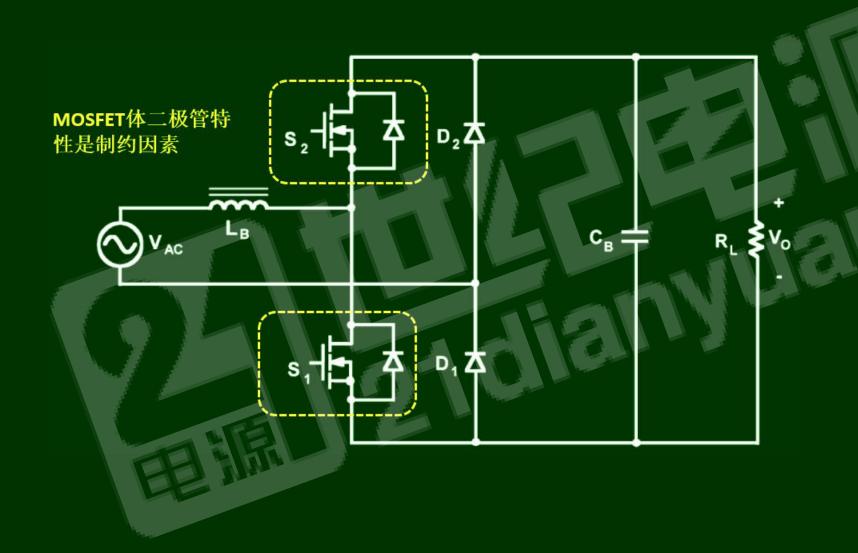


通道1: SR MOS漏源电压Vds (黄色, 20V/DIV) 通道2: SR MOS门极驱动Vgs (绿色, 5V/DIV)

> 原边高压MOSFET驱动电阻 Rgon=100欧姆

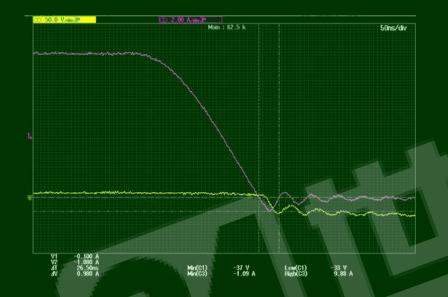


# 超结MOSFET应用在图腾无桥PFC中的问题?





#### SiC MOSFET体二极管反向恢复特性



#### **SIC MOSFET**

650V/120 mOhm

CH1: VDS 50V/div

CH3: ISD 2A/div

Time: 50ns/div

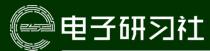
di<sub>F</sub>/dt=100A/us

VDD=50V

IF=10A



Forward voltage	V <sub>SD</sub> *3	V <sub>GS</sub> = 0V, I <sub>S</sub> = 10A		4.3	, <u>-</u>	٧
Reverse recovery time	t <sub>rr</sub> '3		<b>E</b>	33	-	ns
Reverse recovery charge	Q <sub>m</sub> '3	I <sub>F</sub> = 10A, V <sub>R</sub> = 400V di/dt = 160A/µs	1.7	53		nC
Peak reverse recovery current	lum,3		8#8	3.0	*	Α



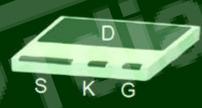
#### Cascade GaN HEMT反向特性

# transphorm

TPH3206LD

Reverse	operation					
Is	Reverse Current	-	-	12	Α	V <sub>GS</sub> =0 V, T <sub>c</sub> =100 °C
V <sub>SD</sub>	Reverse Voltage	•	2.2 3.6		V	V <sub>GS</sub> =0 V, I <sub>S</sub> =11 A, T <sub>J</sub> =25 °C V <sub>GS</sub> =0 V, I <sub>S</sub> =11 A, T <sub>J</sub> =175 °C
V <sub>SD</sub>	Reverse Voltage		1.48		V	V <sub>GS</sub> =0 V, I <sub>S</sub> =5.5 A, T <sub>J</sub> =25 °C
t <sub>rr</sub>	Reverse Recovery Time		17		ns	I <sub>S</sub> =11 A, V <sub>DD</sub> =400 V, di/dt =2000A/μs,
Q <sub>rr</sub>	Reverse Recovery Charge	-	54	-	nC	T <sub>J</sub> =25 °C

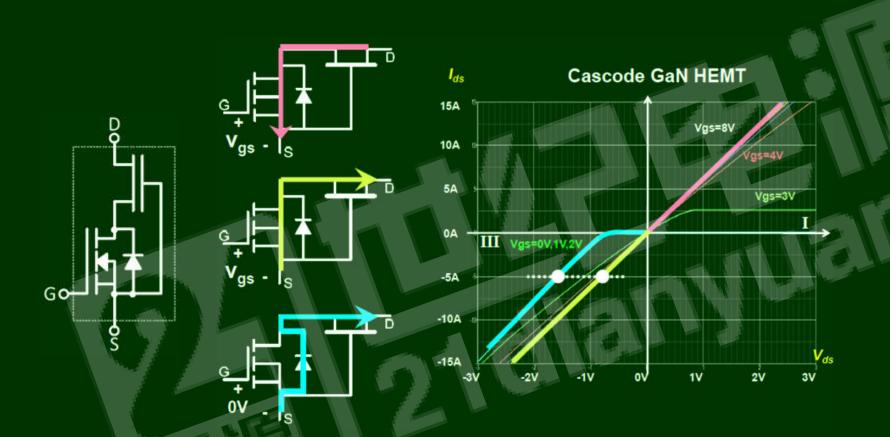


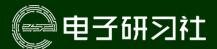


8x8 PQFN Package (bottom view)



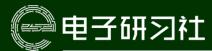
#### Cascade GaN HEMT反向特性



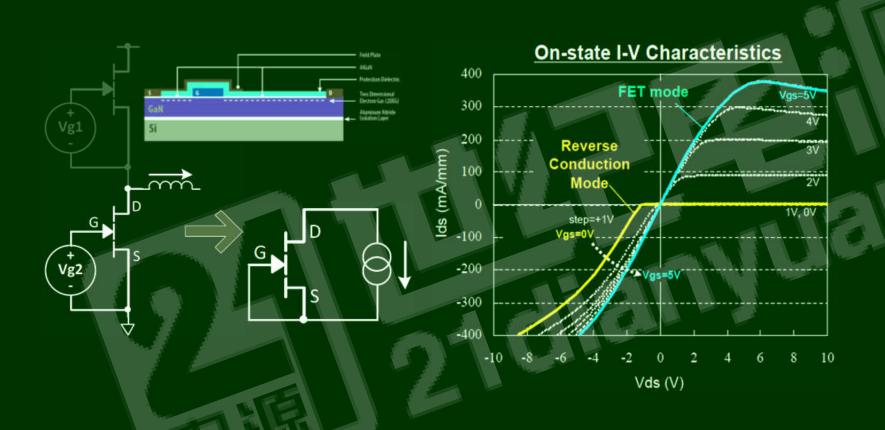


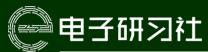
#### Cascade GaN HEMT 和SJ MOS体二极管反向恢复对比





# GaN HEMT(E-Mode ) 反向特性





#### GaN HEMT(E-Mode )反向特性

#### **Panasonic**

PGA26E19BV

Source-drain forward voltage	VSD	VGS=0V,ISD=5A	2.6	V
Reverse recovery charge	Qrr	VDS=400V, ISD=5A, di/dt=400A/us	26	nC

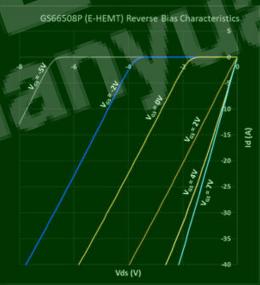


GS66508T

Top cooled 650V enhancement mode GaN transistor

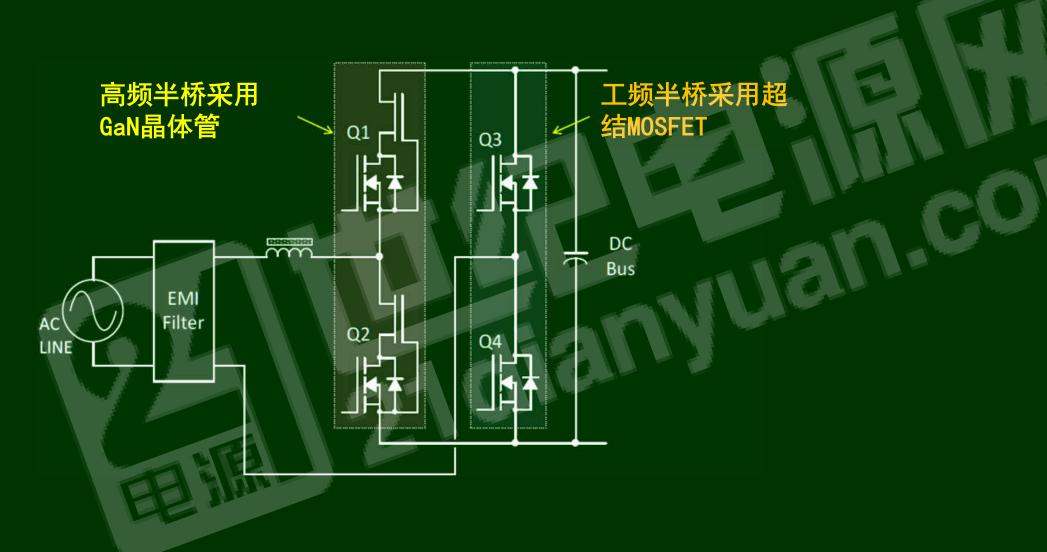
#### **Features**

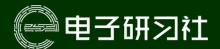
- 650V enhancement mode power switch
- Top cooled configuration
- Ultra low FOM Island Technology™ die
- Low inductance GaNPX<sup>™</sup> package
- Reverse current capability
- Integral source sense
- Dual gate pads for optimal board layout
- Zero reverse recovery loss





#### GaN晶体管和SJ MOS组合用于图腾无桥PFC





# GaN晶体管和SJ MOS组合用于图腾无桥PFC

