Silicon Carbide Power MOSFET 650V N-Channel MOS

■ Applications

• Solar Inverters

• Switch Mode Power Supplies

• High Voltage DC/DC Converters

• Battery Chargers

• Motor Drives

• Pulsed Power applications

■ Features

• High Blocking Voltage with Low On-Resistance

• High Speed Switching with Low Capacitances

• Fast intrinsic diode with low reverse recovery (Qrr)

• AEC-Q101 Qualified

■ Product Summary

V_{DS}	650	V
I_D	77	A
$R_{DS(ON)}$,Typ@20V	30	mΩ
Q_g	98	nC

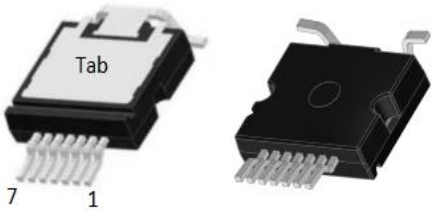
■ Benefits

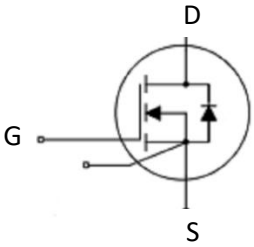
• Higher System Efficiency

• Reduced Cooling Requirements

• Increased Power Density

• Increased System Switching Frequency





Gate： Pin1

Drain： Tab

Source： Pin3~7

Driver Source：

T²PAK-7

Marking	Package	Packaging	Min. package quantity
MLT3C030R065A	T²PAK-7	Tape & Reel	500

■ Absolute Maximum Ratings（Tc=25℃ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	- 5/+20	V
Recommended operational values	V_{GSop}	- 4/+18	V
Continuous Drain Current Tc=25℃ (Note 1)	I_D	77	A
Continuous Drain Current Tc=100℃ (Note 1)		54	A
Drain Current-Pulsed (Note 1)	I_{DM}	230	A
Total Dissipation	P_D	294	W
Junction Temperature	T_j	175	℃
Storage Temperature	T_{stg}	- 55~175	℃

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

■ Thermal Characteristics

Parameter	Symbol	Max	Unit
Maximum Junction-to-Case	$R_{\theta JC}$	0.52	℃/W
Maximum Junction-to-Ambient	$R_{\theta JA}$	50	℃/W

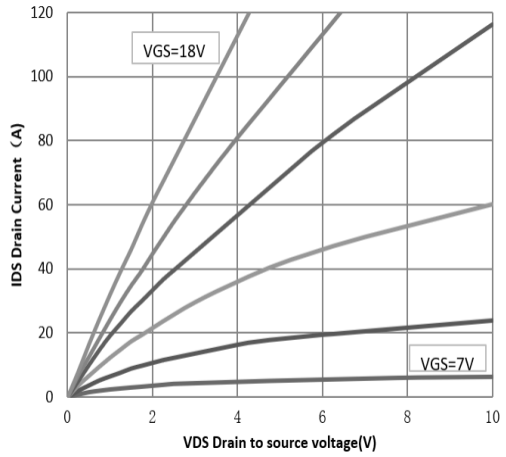
Note 1：Ensure that the channel temperature does not exceed 175℃.

Note：This transistor is sensitive to electrostatic discharge and should be handled with care.

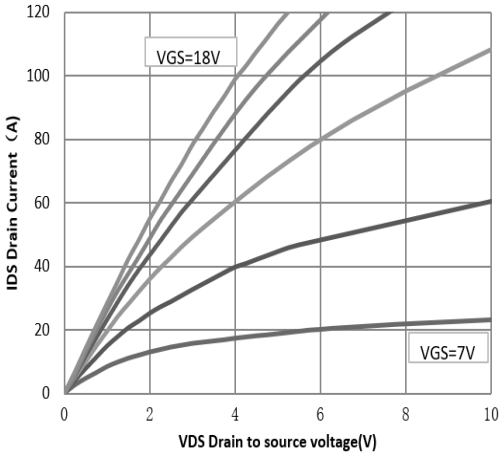
■ Electrical Characteristics（Tc=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Parameters						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=100uA	650	-	-	V
Drain-Source Leakage Current	I_{DSS}	VDS=650V,VGS=0V	-	-	100	uA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	200	nA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS}=V_{DS},I_D=10mA	2.0	2.8	4.0	V
Drain-Source On Resistance	$R_{DS(ON)}$	V_{GS}=18V,I_D=30A	-	30	45	mΩ
		Tj=150°C	-	33	-	
Transconductance	g_{fs}	V_{GS}=20V,I_D=33.5A	-	21		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS}=400V,V_{GS}=0V, f=1.0MHz	-	2330	-	pF
Output Capacitance	C_{oss}		-	227	-	pF
Reverse Transfer Capacitance	C_{rss}		-	13	-	pF
Gate Resistance	R_g	f=1.0MHz open drain	-	5.1	-	Ω
Switching Paramters						
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=400V,I_D=33.5A, V_{GS}=-4/18V,R_G=2.5Ω Timing relative to V_{DS} L=59uH	-	12	-	ns
Turn-On Rise Time	t_r		-	18	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	33	-	ns
Turn-Off Rise Time	t_f		-	9	-	ns
Turn-On Switching Energy	E_{ON}		-	71	-	uJ
Turn-Off Switching Energy	E_{OFF}		-	84	-	
Total Gate Charge	Q_g	V_{DD}=400V,I_D=33.5A, V_{GS}=-4/18V	-	28	-	nC
Gate-Source Charge	Q_{gs}		-	26	-	nC
Gate-Drain Charge	Q_{gd}		-	98	-	nC
Source-Drain Characteristics						
Diode Forward Voltage	V_{sd}	V_{GS}=-4V,I_S=20A	-	3.8	6	V
Continuous Diode Forward Curren	I_S	T_C=25℃	-	-	77	A
Reverse Recovery Time	t_{rr}	V_{GS}=-4V,I_{SD}=33.5A V_R=400V di/dt=1600A/us	-	19.5	-	ns
Reverse Recovery Charge	Q_{rr}		-	218	-	nC
Peak Reverse Recovey Current	I_{mm}		-	22	-	A

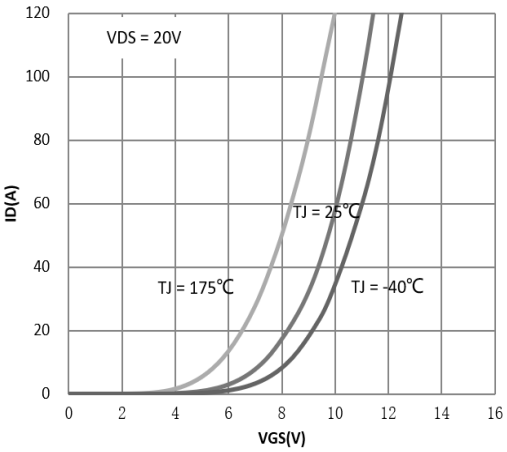
■ Characteristics Curves



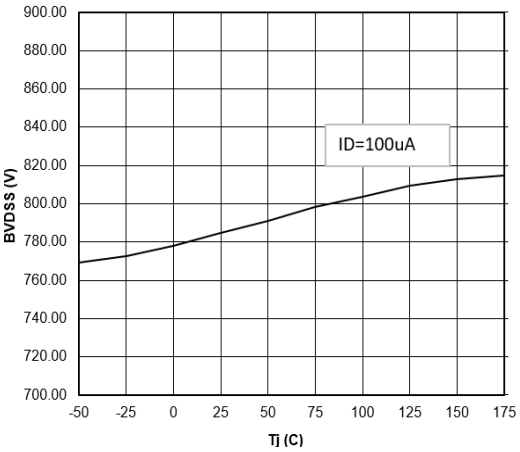
Output Characteritsics T_J=25℃



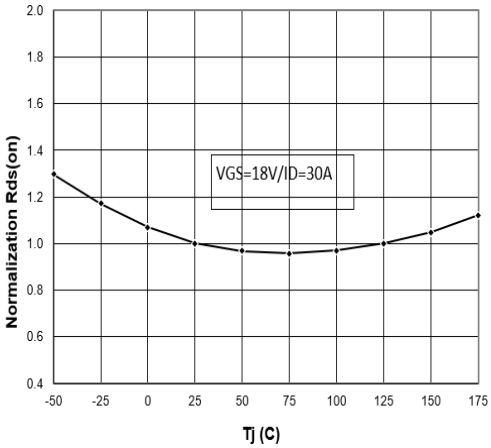
Output Characteritsics T_J=175℃



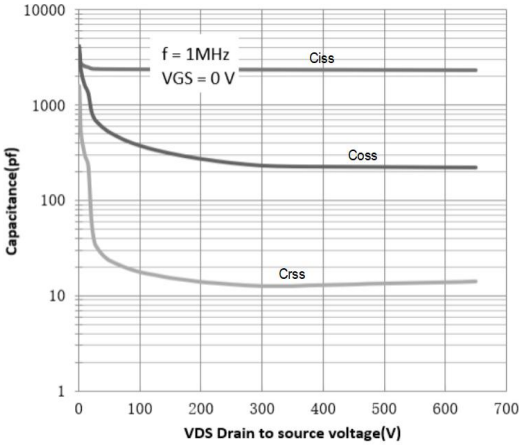
Transfer Characteritsics



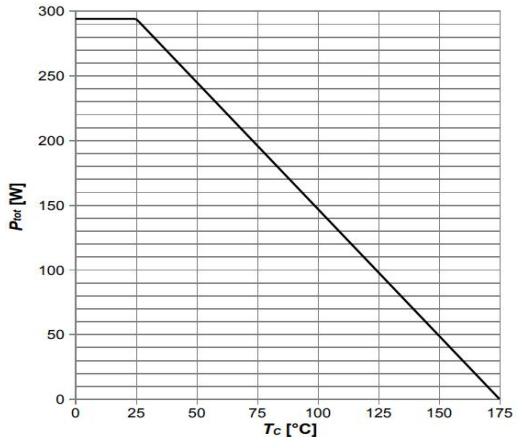
BVDSS vs Temperature



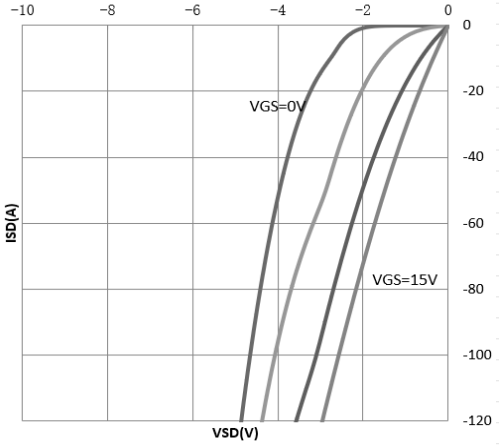
Normalized On-Resistance vs. Temperature



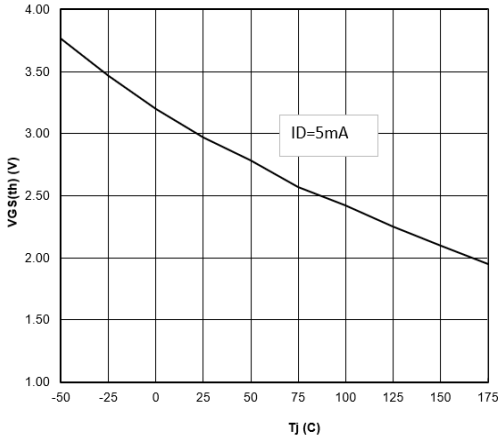
Capacitance



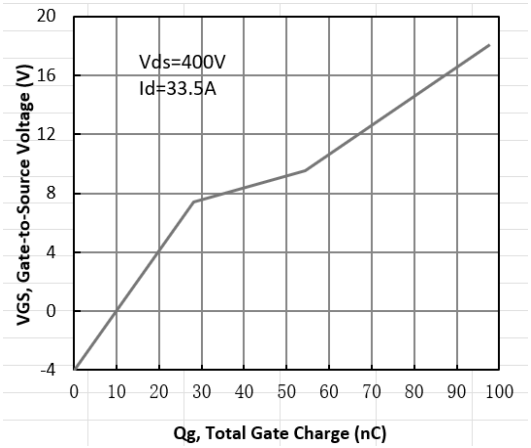
Power Dissipation Derating



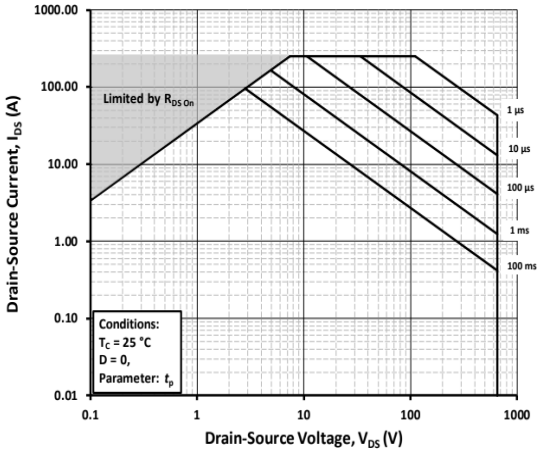
Source-Drain Diode Characteritsics



Threshold Voltage vs. Temperature



Gate Charge Waveform

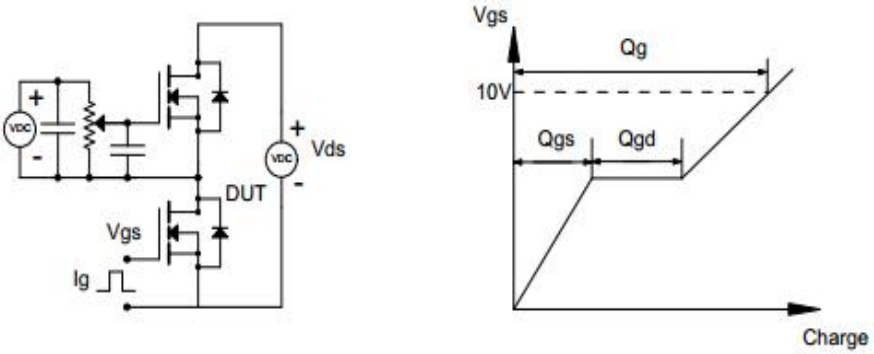


Safe Operating Area

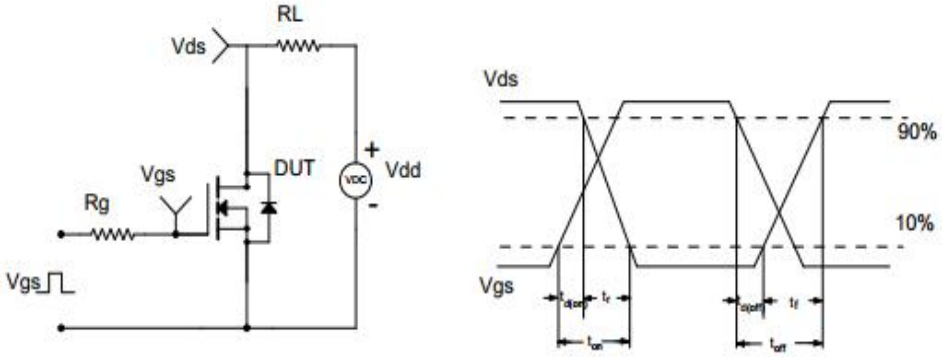
Note：The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

■ Test Circuit & Waveform

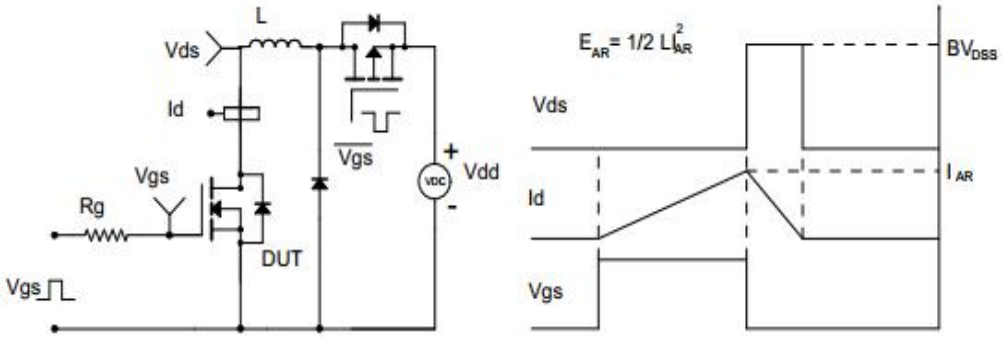
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveform



■ T²PAK-7 Package Dimensions

Unit：mm

Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	3.4	3.5	3.6	e		1.27	
b	0.5	0.6	0.7	L	18	18.58	19
b1	0.7	0.8	0.9	L1	4.44	4.54	4.64
c	0.4	0.5	0.6	L2	1.97	2.52	2.97
c1	0.4	0.5	0.6	L3	0.8	0.9	0.98
D	13.9	14	14.1	L4	2.14	2.24	2.34
D1	13.85	14	14.15	L5		3.04	
D2	12.3	12.4	12.5	L6	2.38	2.48	2.58
D3	4.45	4.5	4.55	T1		0.6	
E	11.7	11.8	11.9	T2		1	
E1	5.46	5.56	5.66	k	0.075	0.125	0.175